Application of Supercapacitor

in Electrical Energy Storage System

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Summary

Understanding the supercapacitor characteristics is mandatory to the application of supercapacitor. In order to do so, an electric circuit model to describe the performance of supercapacitor has to be constructed. The basis of supercapacitor modeling is the parameter acquisition itself, which poses a challenge due to difference in parameter values using different acquisition methods. A series of experiments were done and it was determined that only the AC Electrochemical Impedance Spectroscopy (EIS) and constant current pulse methods were reliable parameter acquisition methodology.

It was discovered that the Equivalent Series Resistance (ESR) of the supercapacitor obtained through the constant current pulse method varies at different point of data acquisition. A novel method is presented which allows the conversion of DC ESR in time domain to the frequency domain. Doing so allows the comparison of AC and DC ESR, which were close in value. This ultimately enables the unification of ESR values: There shouldn't be terms such as AC or DC ESR, but an ESR at stated frequency.

It was experimentally proven that the supercapacitor ESR and capacitance increases with its energy level, which is in line with general findings and knowledge. In order to model the transient characteristics of supercapacitor without taking into account redistribution effect, a modified single branch Resistor-Capacitor (RC) model was proposed, which reflects the change in capacitance and ESR with capacitor voltage. The simulation result of the model is in close proximity of the experimental results, which prove the effectiveness of the model.

With decent understanding of supercapacitor behavior, a bidirectional hexa-mode buck-boost converter was investigated for implementation with the supercapacitor to achieve peak load shaving as well as Uninterruptible Power Supply (UPS) functionalities. Due to the need to operate in both buck-boost and boost modes, a tri-state hybrid mode was proposed to bridge the buck-boost and boost modes. It was proven experimentally that the implementation of hybrid mode can bridge both the modes well. The hexa-mode Switch Mode Power Supply (SMPS) was used to implement a supercapacitor based offline UPS for Hard Disk Drive (HDD). Simulation of real life applications was performed using the programmable electronic load and proves that the hexa-mode SMPS was very versatile in operation and could implement active peak load shaving as well. This SMPS has vast applications especially for low voltage load applications.

List of Abbreviations

Abbreviations	Terms
CCM	Constant Current Mode
DAQ	Data Acquisition
DFT	Discrete Fourier Transform
EDLC	Electric Double Layer Capacitor
EIS	Electrochemical Impedance Spectrometry
ESR	Equivalent Series Resistance
FOH	First Order Hold
HEV	Hybrid Electric Vehicle
HDD	Hard Disk Drive
IEC	International Electrotechnical Commission
NiCd	Nickel Cadmium
NiMH	Nickel Metal Hydride
PEV	Pure Electric Vehicle
RAID	Redundant Array of Independent Disk
SDRAM	Synchronous Dynamic Random Access Memory
SMPS	Switch Mode Power Supply
SOC	State Of Charge
SSD	Solid State Drive
UPS	Uninterruptible Power Supply
ZOH	Zero Order Hold
ZMCP	Zero Maintenance Cache Protection

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Chapter 1

Introduction

1.1 Background

Supercapacitor, or ultracapacitor, is a capacitor with exceptionally large electrical energy storage capacity. It behaves like a typical electrolytic capacitor but with much higher energy density. 5000F supercapacitors are readily available commercially whereas electrolytic capacitors still hover in the milli-Farad range. It is reported that the supercapacitor has up to 1000 times the capacitance per unit volume compared to a conventional electrolytic capacitor [1]. The increased energy density allows the supercapacitor to absorb/ provide power for a significantly longer period of time as compared to the electrolytic capacitor, which gives it new roles in power management and electrical storage.

The supercapacitor was first discovered by General Electric Engineers experimenting with devices using porous carbon electrodes [2]. The technology has been rediscovered several times ever since, but none has been successful in market penetration. It was only during the mid 1990s that various technological breakthroughs allowed both the rapid improvement in performance and reduction in price. The rapidly decreasing price can be observed in Figure 1. The supercapacitor market has henceforth become increasingly popular and competitive with the inclusion of more companies that offer such products. Supercapacitor has since become widely available as an electrical energy storage device.

Figure 1: Price trend of supercapacitor in the last 15 years [3]

1.2 Supercapacitor: Electric Double Layer Capacitor

A typical supercapacitor is known as the Electric Double Layer Capacitor (EDLC), whose properties are based on the double layer capacitance between the interface of a solid conductor and an electrolyte. The structure consists of two active carbon electrodes and a separator immersed with electrolyte, as shown in Figure 2. The electrodes are made up of a metallic collector coated with activated carbon, which provide high surface area to the device. As a matter of fact, activated carbon could achieve a surface area of $2750m^2$ in just a gram of material. The extraordinary large capacitance of the EDLC is mainly due to the use of activated carbon. The electrodes are then separated by a membrane to prevent physical contact. The composite would then be rolled or folded according to the case size.

The EDLC operates like a typical electrolytic capacitor, as it utilizes physical means (charge separation) to store charge. As such, it endures little degradation through each charge/discharge cycle, allowing it to achieve charge cycles of 500,000 – 1,000,000 cycles.

Due to the physical nature of the supercapacitor charge storage, both the charge and discharge processes are equally fast. This imparts the advantage of high power capability and therefore high power density to the EDLC. However, due to the EDLC structure, the breakdown voltage is low, typically a maximum of 2.7V. As a result, although the supercapacitor energy capacity is higher than that of electrolytic capacitors, its energy density is lower than that of chemical batteries.

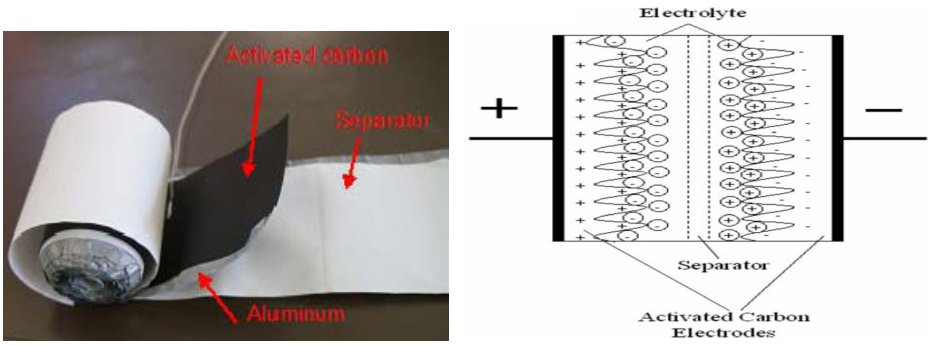

Figure 2: An EDLC dissected (left) and cross sectional view (right)

1.3 Supercapacitor: Pseudo Capacitor

The pseudo capacitor is a new inclusion in the family of supercapacitor. It has structure and characteristics similar to the EDLC, but differs from EDLC in that it utilizes a metal oxide rather than an activated carbon for electrode material. The pseudo capacitor has higher potential for larger energy density than the EDLC. The activated carbon in the EDLC utilized surface area for energy storage, thus limiting potential energy density. The metal oxide technology of the pseudo capacitor is used for electrochemical reaction alike the battery for energy storage, therefore improving energy density. Companies such as Nesscap have successfully developed Pseudo Capacitors which can hold 80% more energy than an

equivalent sized EDLC. The major advantage of this type of capacitor is that its energy density comparable to that of lithium ion batteries.

Due to the chemical reactions involved in charging and discharging, the Pseudo capacitor has much lower charge cycles of 50,000. In addition, due to the chemical reactions, its response is slower than the EDLC. Thus, while Pseudo Capacitor has higher energy density than the EDLC, the slower response and lesser charge cycles negated the advantage. Depending on applications, in particular applications which do not experience much deep charge cycles, one may however find Pseudo Capacitor more applicable. Pseudo Capacitor is much less popular than the EDLC; therefore the focus of the thesis is on the EDLC. The term "supercapacitor" used henceforth refers to the EDLC.

1.4 Latest Trends in Supercapacitor

Figure 3 illustrates the characteristic of a supercapacitor developed by Dalian University of Technology, Nanotek Instruments and Angstron Materials. It is featured as the highest energy and power density for supercapacitor today. It is rated at 85.6 Wh/Kg at room temperature and 136Wh.Kg at 80 °C, measured at a current density of 1A/g [4]. These put the graphene supercapacitor comparable to that of Nickel Metal Hydride (NiMH) battery where energy density is concerned, as observed in Table I. It is made possible by preparing curved graphene sheets. Also, the curved morphology allows the use of environmentally benign ionic liquids capable of operating at above 4V. All these pointed to a distinct future: With the rapid improvement and falling price of supercapacitors, it will find more applications rapidly.

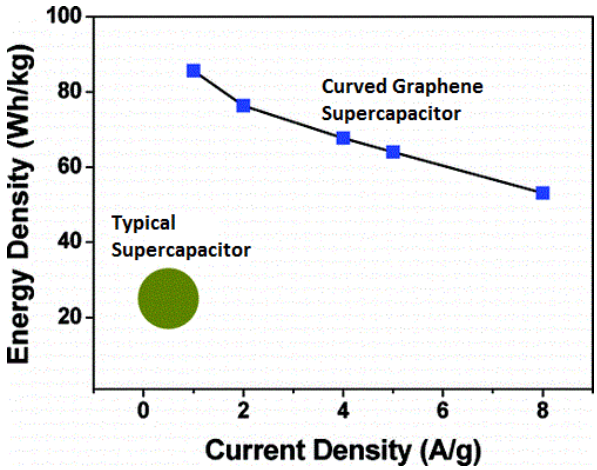

Figure 3: Energy and current density of graphene based supercapacitor [5]

1.5 Supercapacitor as An Energy Storage Device

Energy storage devices are used to store some energy that can be released at a later time to perform some useful operation. A good energy storage device should be one that has very high energy density, so that the volume and weight efficiency is high. Therefore, where electrical energy is concerned, the most popular form of energy storage would be the chemical storage device. Chemical storage devices are aplenty, such as the fuel cell and battery. While fuel cell has the highest energy density, the most popular electrical storage device is however the battery.

Some popular rechargeable batteries today include the Lithium Polymer battery, Lead Acid battery as well as NiMH battery. Summarized in Table I, the Lithium Polymer battery has the highest energy density as well excellent round trip efficiency. Thus, the Lithium Polymer battery will be gradually replacing NiMH and Lead-acid batteries in many applications, some of which include mobile devices as well as automotive vehicles. In comparison, commercially available supercapacitor has the lowest energy density but it is unmatched in

power density as well as recharge cycles. These characteristics bestow a new role onto supercapacitor as an electric storage device.

Table I: Characteristic of different types of energy storage device [6-7]

Type	Voltage	Energy density			Power	Efficiency	E/$	Cycles
	(V)	(MJ/kg)	(Wh/kg)	(Wh/L)	(W/kg)	(%)	(Wh/$)	(#)
Lead-acid	2.1	0.11-0.14	30-40	60-75	180	70%-92%	8-May	500-800
NiMH	1.2	0.11-0.29	30-80	140-300	250-1000	66%	1.37	1000
Lithium polymer	3.7	0.47-0.72	130-200	300	3000+	99%	2.8-5.0	500~1000
Maxwell EDLC Supercapacitor	2.7	0.022	6	6	15000	99%	30	1000000
Prototype EDLC	>4	0.31-0.49	86-136		32000	~99%		~1000000

Where electrical energy storage devices are concerned, categorization often involves the usage of ragone plot. The ragone plot takes into account energy storage capacity in Wh/Kg against the pulse power capacity in W/Kg. This chart is used to compare the relative advantages of one's energy storage technology against others. Figure 4 illustrates the relative position of commercially available supercapacitor in the ragone plot.

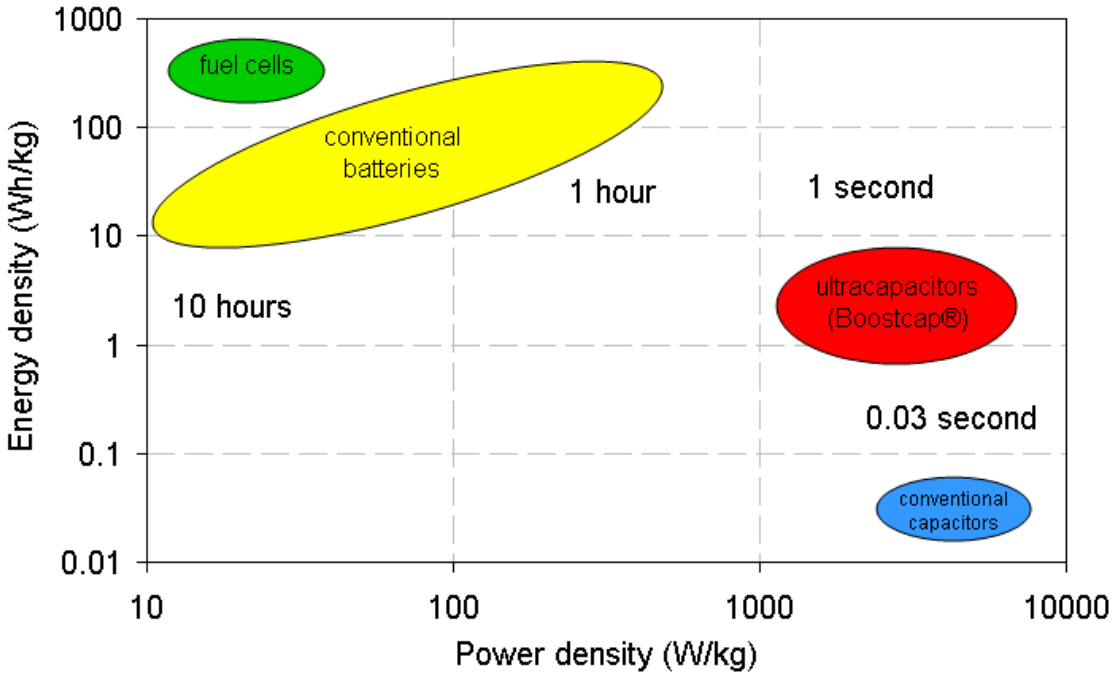

Figure 4: Ragone chart for various energy storage devices [7]

Supercapacitor has many important characteristics that made its application very desirable. Unlike batteries, supercapacitors can operate optimally at low temperatures [8]. It is easily understood why one of the first uses of supercapacitor included military projects to start the engines of military tanks, especially in cold weathers. The practically unlimited charge cycles coupled with exceptionally high power density also saw supercapacitor as an ideal energy buffer that performed peak load shaving for existing systems. Peak load shaving is a process that utilized the energy buffer to reduce power demand of the main energy source, which had been known to improve system efficiency and prolong lifespan of batteries [9].

The main reason why these are possible is because supercapacitor stores energy through physical electrostatic charge. It explains why supercapacitors can be charged as quickly as they can be discharged. This is spectacular as no chemistry based battery can achieve this: Battery chemical reactions are either endothermic (Ni-Cd) or exothermic (Ni-Mh). Battery charging is very sensitive to temperature, which does not allow the chemical reactions to occur at any rate the user wants without damage [10]. Therefore, the charge and discharge capability of chemical batteries vary widely.

Typically, the charge rate of chemical batteries is low compared to the discharge rate. As such, this is one of the biggest advantages of supercapacitor that renders it the most popular solution to any peak load shaving devices. Having physical charge storage mechanism also ensures that supercapacitors inherit very fast response time to power demand as compared to chemical batteries. Most battery chemical reactions not only limit power density but also delay the response time to power demand.

As peak load shaving devices are likely to operate much more often than the main energy source, the peak load energy storage device has to undergo many charge cycles compared to

the main energy source. This is uniquely suited for supercapacitors as it is able to undergo many charge cycles with little degradation of performance. With the various distinct advantages, supercapacitors are deemed to have much potential to be used in applications such as the hybrid/electric vehicles, mobile phones, micro-grids etc.

1.6 Issues with Supercapacitor

Although supercapacitor technology is under rapid development today, there are still many issues concerned in its application.

1.6.1 Supercapacitor Parameter Issues

To fully understand supercapacitor behavior, one would need to comprehend the relevant parameters such as capacitance and ESR. Only with reliable parameter values can be used to describe the performance of the supercapacitor. This is however, not an easy task as these crucial parameters are known to vary due to temperature as well as operating conditions (voltage, current, frequency and temperature). One other important issue is that, parameter measurement methods are aplenty and each method acquired parameter value different from that of other methods. These causes the establishment of measurement standards such as the IEC 62391 which dictates the supercapacitor measurement conditions and procedures, so that supercapacitor measured under this platform can be reference and is comparable to another that was measured in the same platform. However, the measurement standards can be vastly different from the intended usage, rendering the parameters obtained questionable. Of

importance is however, the reliable and accurate parameter value acquisition that is obtained under the application operating conditions.

1.6.2 Electric models of Supercapacitor

The electric model of supercapacitor serves as an analytical understanding of supercapacitor performance. However, construction of the supercapacitor model is difficult as it must be accurate in describing long term effects such as the supercapacitor charge equalization effect as well as long term discharge. These give rise to many analytical methods to obtain multi-branch supercapacitor models, which are time consuming and demand much effort. In many applications, only the transient performance of supercapacitor is needed. The basic RC model is easy to implement but lacks the ability to achieve close approximation of experimental data even in the transient region. Thus, one may have to consider multi-branch models and the associated long term effects even though only the transient performance is of concern.

1.7 Voltage Regulators for Supercapacitor Applications

Most supercapacitor applications leverage on its fast charge, fast discharge and/or near unlimited charge cycles. However, the application of supercapacitor is not straight forward. Unlike chemical batteries, supercapacitor charge storage is dictated by its voltage, as denoted by

$$Q = V \bullet C \quad (1)$$

It indicates that the supercapacitor useful State of Charge (SOC) is from 0 V to the maximum voltage rating. It causes difficulty in the voltage regulation of supercapacitor.

Applications of chemical battery involve the use of voltage regulators as well. However, its useful SOC is within a relatively small voltage window, 3.0 – 4.2V in the case of Lithium Ion battery [11]. Thus, voltage regulation is less difficult in this application due to lower magnitude in voltage fluctuation as compared to supercapacitor. Therefore, voltage regulators designed for chemical batteries cannot be used directly for applications of supercapacitor. Voltage regulators of different topologies have to be employed to achieve voltage stabilization for supercapacitor.

Focus of Thesis

The focus of this thesis is to investigate the supercapacitor performance and the associated parameter acquisition methods, so as to derive a supercapacitor model that is capable of describing the transient performance of supercapacitor. Also, the application of supercapacitor through SMPS voltage regulators will be discussed to implement a highly versatile SMPS that allow supercapacitors to be implemented effectively as an energy storage element. In order to achieve so, two issues have to be tackled, namely:

1. Identifying the most reliable supercapacitor parameter acquisition method amongst other methods.
2. Selection of bidirectional SMPS to maintain constant output voltage.

Thesis Contributions:

The contributions of the thesis are as follows.

1. By analyzing and performing experiments, both reliable and unreliable supercapacitor parameter acquisition methods are identified. The related experimental methods and results are also introduced and analyzed;
2. A method allowing the conversion of DC ESR to the frequency domain makes the comparison with AC ESR be possible. It allows the unification of supercapacitor ESR.
3. A modified single branch RC model that reflects variation in capacitance and ESR with change in voltage is proposed and discussed. Compared with the basic RC model, results from the modified single branch RC model simulation proved that it is closer to the experimental findings where transient performance is concerned.
4. A tri-state hybrid mode is incorporated into the bidirectional hexa-mode converter, which bridges the buck-boost state to the boost state. The buck-boost and boost modes are subsets of the hybrid mode.

Thesis Organization

The thesis consists of several divisions, as shown below.

Chapter 1: Introduction of Supercapacitor

This chapter is an introduction to supercapacitor. The various issues as well as electric modeling are discussed.

Chapter 2: Supercapacitor as Electrical Energy Storage Element

This chapter is a summary of literature survey on the current and potential applications of supercapacitor as an electrical energy storage device. It emphasizes the importance and popularity of SMPS based voltage regulators in the application of supercapacitor.

Chapter 3: Characterization of Supercapacitor

This chapter describes how supercapacitor parameters can be acquired as well as the difference in the various methodologies. Two methods are justified as reliable using experimental values, the values which were also used to implement the proposed supercapacitor model. Unification of AC and DC ESR values is achieved by identifying frequency values in the DC ESR.

Chapter 4: Bidirectional SMPS Converters

Chapter 4 discusses and analyzes bidirectional SMPS topologies for the implementation of supercapacitor as an energy buffer, otherwise which is impossible due to the rapid fluctuation of supercapacitor voltage. The bidirectional hexa-mode buck-boost converter as well as the accompanying hybrid mode is introduced here.

Chapter 5: Practical Implementation of Bidirectional SMPS with Supercapacitor

This chapter describes the algorithm used to implement the hexa-mode converter as well as the experimental hardware setup. The converter was built and went through a number of load testing conditions to prove that the converter is indeed as versatile as mentioned. In addition, it was made to implement an off-line UPS functionality with a HDD.

Chapter 6 presents the thesis conclusions and future works for supercapacitors.

Chapter 2

Applying Supercapacitor as Electrical Energy Storage Element

2.1 Introduction

Many types of electrical equipments today can benefit from a highly efficient energy buffer. In many scenarios, the supercapacitor can be integrated into the system to implement the energy buffer. Some of such applications include automobile, micro-grid, green power generation, mobile devices, data storage devices and much more.

2.2 Application of Supercapacitor – Automobile

Some of the most popular applications of supercapacitor include automotive vehicle incorporation. Hybrid Electric Vehicles (HEV) and Pure Electric vehicles (PEV) were gradually popularized over recent years. With much research efforts spent into improving the fuel economy of vehicles, both HEV and PEV represent the one of the important trends of vehicle development.

Both the HEV and PEV contain an electrical machine onboard for propulsion. When the vehicle starts to move off, the initial power required by the motor can be several times that of the average power demand. Deprivation of electrical power during this instant simply imply

sluggish pickup performance. This is a highly challanging task as batteries with high energy density, e.g., lithium battery, are limited in output power capability.

Comparatively, supercapacitor has both superior output and input power capability. The optimization of regenerative braking in vehicles is of much concern, for doing so allows the vehicle's kinetic energy to be saved and utilized at a later moment, reducing energy that is otherwise wasted as heat [12]. As the power delivered during regenerative braking is vast, the high input power capability of supercapacitor makes it exceptionally suitable to achieve significant energy saving and carbon reduction. Therefore, supercapacitor has the potential to play an important role in automobile applications.

Automotive manufacturers such as Honda have been proactive in HEV development. They had developed their own unique supercapacitor in the hope to improve HEV performance, which was also implemented in the Honda FCX. The FCX is primarily a fuel cell powered car. Traditional fuel cell vehicles suffer from slow initial acceleration, which was mainly due to the slow response of fuel cell topology. However, Honda overcame this issue by incorporating supercapacitor as an energy buffer for the vehicle. The final outcome is a FCX which was able to accelerate and decelerate quickly, untypical of a fuel cell powered vehicle [13].

Figure 5: Honda self-developed supercapacitor stack (left) used on the FCX (Right) [13]

A number of researchers have embraced this approach and achieved the same outcome. The main novelty in this approach is to utilize the supercapacitor to deliver power during transient periods when the fuel cell is unable to cope. Being able to do so allows the system to achieve fast response even though the main energy source is slow in response [14]. This role is uniquely suitable for supercapacitor due to the need to experience frequent charge/discharge cycles as well as high power conditions. No other electrical storage devices are capable of such performance. The voltage regulator commonly used by researchers is often of the two quadrant SMPS topology as observed in Figure 6 [14].

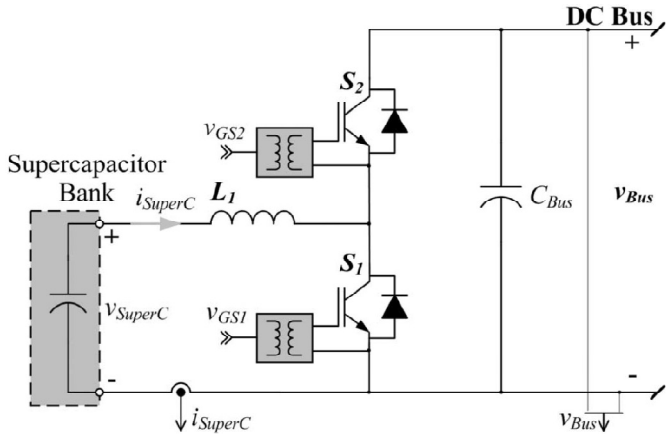

Figure 6: Two quadrant supercapacitor converter [14]

The first production HEV, the Toyota Prius, brought along the regnerative braking feature in an attempt to store energy otherwise wasted as heat in braking. Many car manufacturers followed suit thereafter, and much research had also been directed at developing different regenerative braking topology. Today, almost all HEV and PEV come equipped with regenerative braking as a standard feature whereas conventional gasoline/ diesel powered Internal Combustion Engine (ICE) vehicles such as the Mini Cooper has already started to

incorporate this feature. It was undeniable that regenerative braking is going to be a standard feature in all future production vehicles.

Regenerative braking is the change of propulsion machine to regenerative mode. It produces a braking effect to the vehicle as the vehicle forward momentum is used to produce electrical energy through the machine. Depending on the mass of the vehicle as well as the rate of velocity decrease, vast amounts of electrical energy can be recovered. The magnitude of back-EMF produced by the machine during braking is dependent on the speed of motor shaft, or indirectly the vehicle speed. Therefore, it must be noted that regenerative braking is delivered with much voltage fluctuation.

Harnessing this amount of energy is crucial to both the improvement of fuel economy as well as braking performance. In most HEV and PEV, the regenerated energy is used to charge the auxillary battery directly. However, battery charge rates are often severely limited due to chemical reactions taking pace inside the battery to store electrical energy. In vehicles that are unable to absorb the huge amount of power, the excess electrical energy is often dissipitated through resistors as heat. A popular method include using conventional braking to further decelerate the vehicle once the braking power exceeds the system's capability to absorb power. An energy buffer capable of absorbing this huge amount of energy is ideal to improve the energy efficiency of regenerative braking. The supercapacitor is uniquely suited for this role as its capabiity to absorb energy far exceeds that of the battery.

2.3 Application of Supercapacitor – Mobile Devices

Supercapacitors can take on many different physical forms. Cap-XX has been active in promoting thin and small supercapacitor which can be applied in applications which had

severe space constraint. Figure 7 illustrates such a supercapacitor installed in a mobile phone as outlined in red.

Some recent mobile phones have high quality xenon flash inbuilt into the phone to enable good photo quality when light is scarce. Xenon flash has traditionally been used on cameras, and consumes much power in an instant. Should the mobile phone have to cater to the power requirement, it would have added unnecessary bulk and weight to the battery, failing which would result in severely shortened battery life.

Some mobile manufacturers have incorporated a supercapacitor into the mobile phone to ease the temporary high power demand. In this application, the supercapacitor performs peak load shaving, as observed in Figure 8. It is shown that with peak load shaving, the battery current is suppressed at a maximum of 0.2A even though the camera flash current may be as high as 4A. Although the battery supplies the entire energy requirement, it does not see high power demand. The supercapacitor voltage experiences a significant fall as a result of supplying energy to the flash. As a result, the battery does not have to be large to cater to temporal high power demands.

Figure 7: Mobile phone with supercapacitor built-in [15]

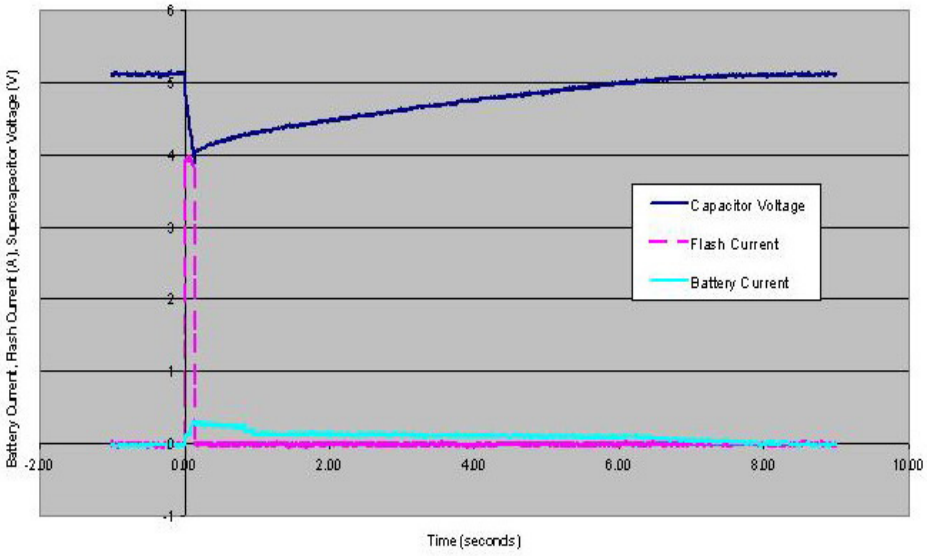

Figure 8: Supercapacitor peak load shaving in mobile phone camera flash [40]

It has also been proven that using supercapacitor as a peak load shaving device can result in much better performance for camera flashes [15]. Therefore, using supercapacitor in mobile phones not only improve battery life but also camera performance. To achieve the peak load shaving operation as observed in Figure 8, it is necessary to incorporate a SMPS.

2.4 Application of Supercapacitor – Micro-Grid

The micro-grid is labeled as a possible next-generation energy network. It comprises of electrical power generation units as well as electrical energy storage components. Popular electrical power generator includes photovoltaic cell, wind turbine, fuel cell and micro-turbine while commonly used electrical energy storage units would be the supercapacitor and battery. As the micro-grids can be inter-connected to the power grid, it is able to supply or demand power from the power grid. At times, this configuration is known as the smart grid. The micro-grid has the capability of reducing carbon emission through green energy

harnessing as well as having the potential of providing self sustainable energy. Thus, it is regarded as a contender for the next generation energy network. [41]

Whilst electrical power can be generated by a combination of any generators, the electrical energy storage units can also comprise of a combination of any batteries or supercapacitors. The Battery Supercapacitor Hybrid Storage (BSHS) is a combination of battery and supercapacitor used in the micro-grid. Due to the higher energy density of the battery, it takes on the role of the main energy storage device while the supercapacitor performs the role of peak load shaving through a SMPS. The BSHS combination is greatly enhanced to handle temporal high power requirements during operation, such as a sudden spike in input power from the electrical power generators. [42]

2.5 Application of Supercapacitor – Data Storage Devices

Supercapacitors opened up a new era of cache protection functionality. Data centers traditionally rely on UPS to cater power to data storage devices whilst the mains power is offline. However, UPS capacity is not only limited but also unable to sustain long periods of operation relying on the batteries alone. To overcome this issue, enterprise Redundant Array of Independent Disks (RAID) controllers contain a Lithium Ion battery which is aimed to sustain the operation of data storage devices for a period of up to 3 days. Whilst this is a good solution, it presented several disadvantages. The first disadvantage is that the system will lose precious data after the battery ran out of charge. Additional disadvantage include periodic change of battery even though the battery may not have been utilized during the period. These incur additional costs and hassle in the long run.

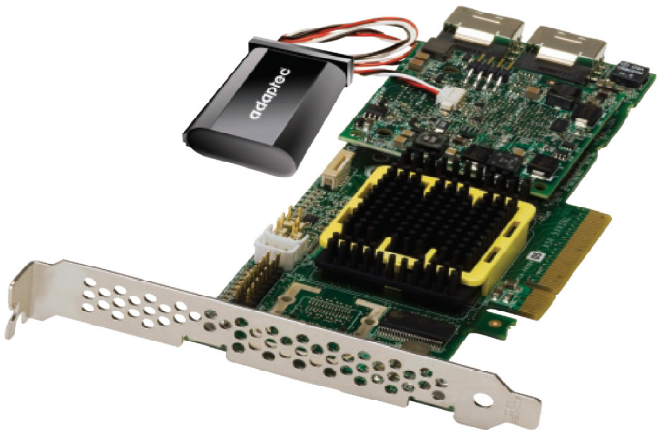

Figure 9: Adaptec 5Z RAID controller with supercapacitor [16]

In recent years, major RAID controller companies have been seen ditching the Lithium Ion batteries for supercapacitors, mainly due to the maintenance-free nature of supercapacitor. Not only is it environmentally friendly, supercapacitors also eliminate the need to replace the Li-Ion battery periodically [17-20]. Adaptec is amongst the earliest to implement the supercapacitor backup system, and calls it Zero-Maintenance Cache Protection (ZMCP).

Under this system, the supercapacitor energy storage kick in the moment mains power is lost to maintain data storage device operation. The data on cache and other volatile memory would be written to the embedded non-volatile flash memory for permanent storage. These operations are accomplished in matters of seconds, during which they are being sustained by the supercapacitor. When the mains power came back on again, the system would recover the cache and memory through the embedded flash memory, and resume operation [21].

The novelty of this system is that the data storage devices can resume original operations even though untouched for years. The system was touted Zero-Maintenance due to the fact that supercapacitors have virtually unlimited charge cycles and suffer little degeneration compared to chemical batteries. A number of such patents had been filed by other companies as well [16].

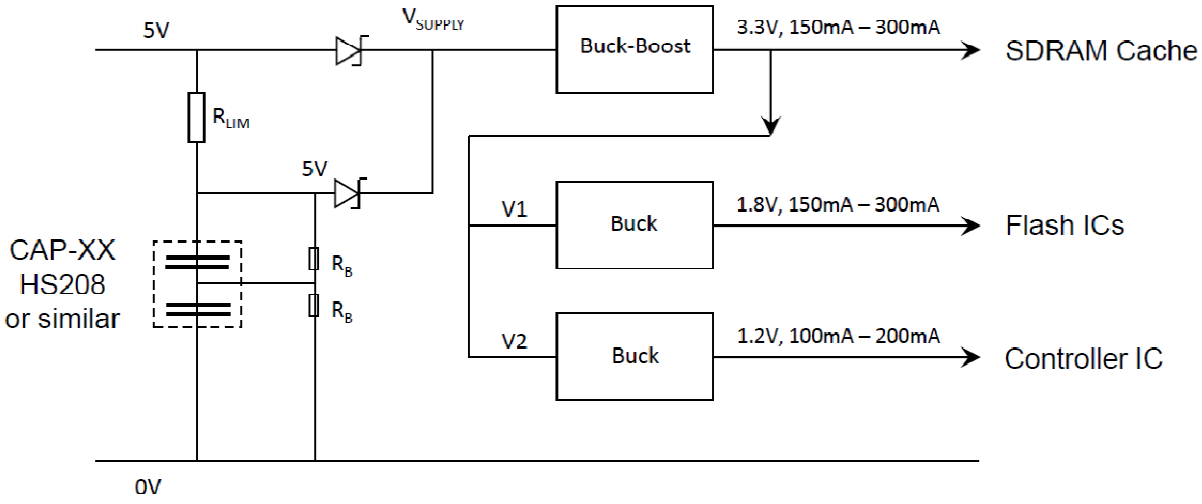

Figure 10: Control topology for supercapacitor SSD SDRAM buffer [22]

In recent years, the Solid State Drive (SSD) has seen much improvement and market penetration. It has the advantage of being fast (in both access time and transfer speed) and free from mechanical devices when compared to conventional HDD. However, early SSDs suffered from limited write cycles as well as poor write performance. As a result, most SSD today have implemented a volatile cache, typically of Synchronous Dynamic Random Access Memory (SDRAM) nature.

The cache primarily deals with metadata which require many writes cycles for every file operation. As the SDRAM is significantly faster than SSD, using it as a cache not only improve the write performance but also reduce the write cycles on the SSD itself. The result is a fast drive in both writing and reading and also improved lifespan for the SSD.

The danger is when a power failure occurs, causing all the data in the cache to be lost. The larger the cache, the more the data loss would be. Companies such as Cap-XX have proposed a solution: Introduce supercapacitors to the SSD as an energy buffer, which provide the SSD

sufficient time to store all data in the cache before powering down. Figure 10 demonstrates the backup power topology using supercapacitor recommended by Cap-XX [22].

It has to be noted that supercapacitor has changed the way energy buffer is implemented for data storage devices. The energy buffer has evolved from the system level UPS, to sub-system RAID UPS, and finally device level UPS. As such, supercapacitors are directly penetrating the data storage industry unlike any energy storage device has done before.

2.6 Chapter Conclusion

The applications of supercapacitor in electrical energy storage are plentiful and yet irreplaceable. Some applications take advantage of the high power density, others utilizes the near infinite charge cycles, or even a combination of both. Supercapacitors can be a revolutionizing element in energy storage system. A number of applications use supercapacitor to complement existing battery as a hybrid energy storage device in order to cope with instantaneous high power demand, such as in mobile phones or micro-grids. In addition, supercapacitors possess much potential to serve as a device energy buffer in the data storage industry. Thus, each SSD may potentially be sold with an inbuilt supercapacitor in the future.

Chapter 3

Characterization of Supercapacitor

3.1 Introduction

In order to apply supercapacitor well, it is advantageous to understand its model well, which is equivalent to understanding the characteristics well. Although there are several methods to acquire supercapacitor parameters, it is unfortunate that supercapacitor parameters differ according to the acquisition method. Small deviation of supercapacitor ESR can result in very different performance.

It is understood that the supercapacitor operational current condition can be quantized into $\mathcal{C}$ ratings. $\mathcal{Q}$, representing a unit of $\mathcal{C}$, is defined in (2). The $\mathcal{C}$ rating cross links all supercapacitor into a single platform that normalized the current operational condition in place of amperes. This way, it is easier to find the equivalent current condition for different supercapacitors of different capacity and current ratings.

$$\mathcal{Q} = \frac{C(V_{\max} - V_{Min})}{3600}, \tag{2}$$

where, C is the capacitance in farads, $(V_{max} - V_{Min})$ is the operating voltage range used for testing and $\mathcal{Q}$ is the resulting charge in ampere-hours.

To verify the performance of supercapacitor, three supercapacitors of different reputable brands and models were used in the experiment, details which were summarized in Table II.

They vary from 20F to 50F in the manufacturer datasheet. Supercapacitors of such values were chosen as a moderate current draw from supercapacitor of such capacity is equivalent to a large current draw from a larger supercapacitor. The $\mathcal{C}$ ratings are summarized in Table II and Table III.

Table II: Q Rating of Supercapacitor samples

	Supercapacitor 1 (50F)	Supercapacitor 2 (20F)	Supercapacitor 3 (50F)
Model	Maxwell BCAP0050 P270	ELNA DZ-2R5D206K8T	Panasonic EECHW0D506
Q	0.0375	0.015	0.0375

Table III: Conversion of current drawn to $\mathcal{C}$ rating

I/A	Supercapacitor 1/ $\mathcal{C}$	Supercapacitor 2/ $\mathcal{C}$	Supercapacitor 3/ $\mathcal{C}$
1	26.7	66.6	26.7
3	80	200	80
5	133.3	333.3	133.3
7	186.6	466.66	186.6

3.2 Classification of Supercapacitor Models

It is necessary to model the supercapacitor in the most appropriate manner to allow simulation results to reflect real world results. Accurate modeling of supercapacitor is difficult as it was discovered that the capacitance suffers variation due to frequency as well as terminal voltage as observed in Figure 11 [23-24]. In addition, ESR of the supercapacitor varies due to operational conditions such as voltage and current ratings. Thus, several models have been proposed to describe the supercapacitor behavior, out of which, the RC and parallel RC branch topology are the most popular variants.

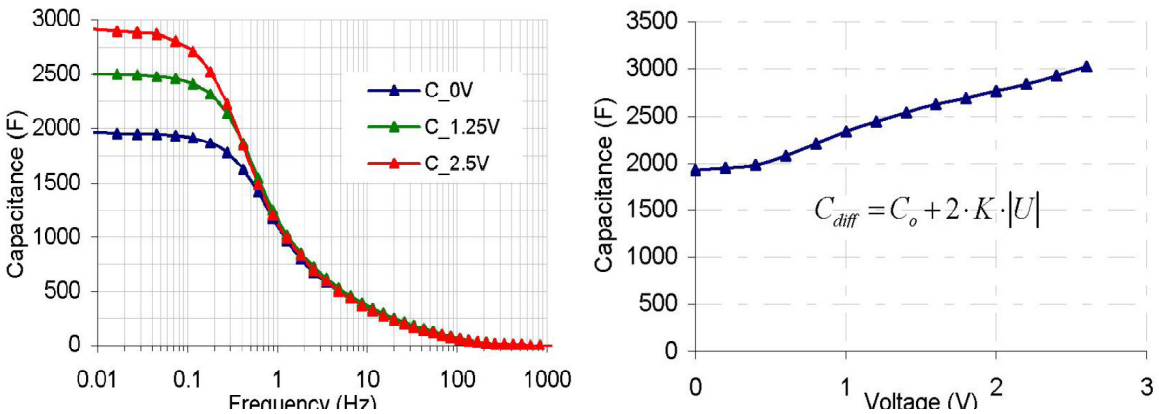

Figure 11: Differential capacitance according to frequency at constant temperature (left) and capacitance as a function of voltage at 0.01 Hz and 20 degree Celsius (right) [24]

3.3 The Basic RC Model

The RC model is the simplest supercapacitor circuit mode [25]. It includes the ESR as a form of parasitic whose effect could be seen during charging and discharging.

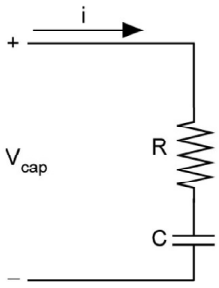

Figure 12: RC equivalent model of supercapacitor

Simple as the RC circuitry may be, Figure 13 shows that it is unable to account for:

1) The supercapacitor gradual voltage drop, which is a prominent phenomenon in all supercapacitor and influences the use of it. It is observed in the Figure 13 during T=40 seconds and T=130 seconds.
2) T=175 to T=250 seconds, where the capacitor voltage is rising.

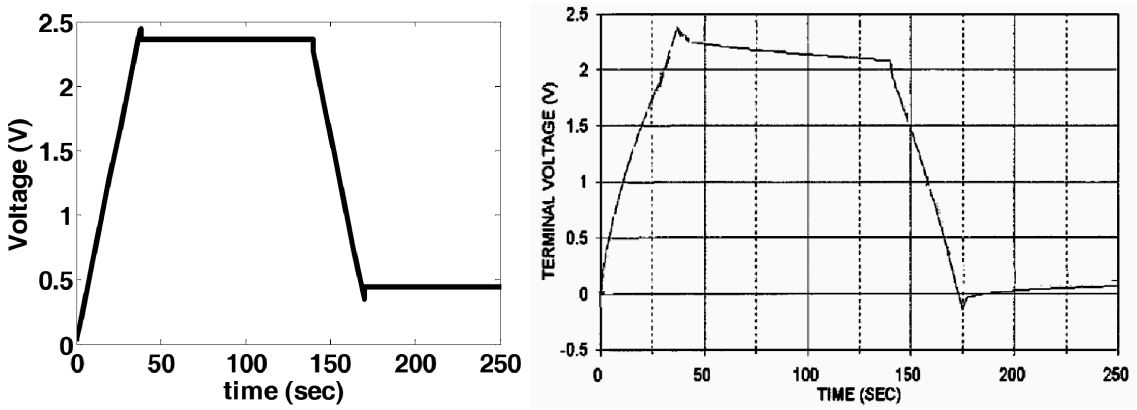

Figure 13: Simulated results (left) and practical results (right) of supercapacitor charging and discharging performance during constant current charge and discharge respectively [25]

Both phenomena are due to the supercapacitor equalization effect, but it cannot be described by the RC model. The supercapacitor equalization effect is the phenomenon in which supercapacitor voltage recovers from the act of charge/discharge. This results in the gradual decrease of voltage after charging and gradual increase of voltage after discharge. Thus, the RC model can only serve as a rough model in describing how the supercapacitor behave where the transient portion is concerned. As observed in Figure 13, the supercapacitor voltage increment is not entirely linear whereas the simulated model reflects a linear voltage increment. This is mainly due to the capacitance change with supercapacitor voltage changes. Thus, even though the long term equalization effect is not taken into consideration, the basic RC model is insufficient to model supercapacitor behavior. The worst case deviation occurs when multiple charge/recharge are performed for long periods of time.

3.4 The Parallel RC Model

The RC parallel branch model serves to simulate the actual supercapacitor behavior during charge and discharge. It is noted that when charging stops, the terminal voltage drops, after which it would stabilize after tens of minutes [25]. To simulate this, a parallel branch model

of different time constants would be able to simulate the charge and discharge process. Theoretically, this model work best with a large number of RC branches. However, in order to simplify the simulation model and yet obtain satisfactory results, the three branch model is widely adapted. Typically one branch would have a time constant in the matter of seconds, which is responsible for the charging and discharging in the seconds range. This is often termed the fast branch. Another branch that dominates supercapacitor performance in the minutes range is termed the middle branch. The slow branch is responsible for the long term characteristic of the supercapacitor in the order of 10 minutes or longer.

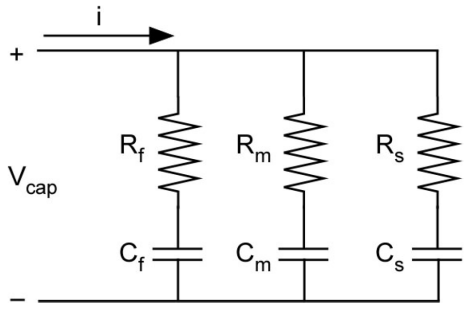

Figure 14: Parallel RC equivalent model of supercapacitor

The model is fairly accurate but had significant errors in the low voltages. This is mainly due to the fact that in the seconds range operation, the middle and slow branch are unable to contribute to the output results significantly, resulting in an equivalent RC circuitry. Its strengths lie in the higher terminal voltage, typically above 40% [26].

The RC parallel branch model can be decomposed as seen in Figure 15, where the order is gradually reduced to a simpler equivalent model [27].

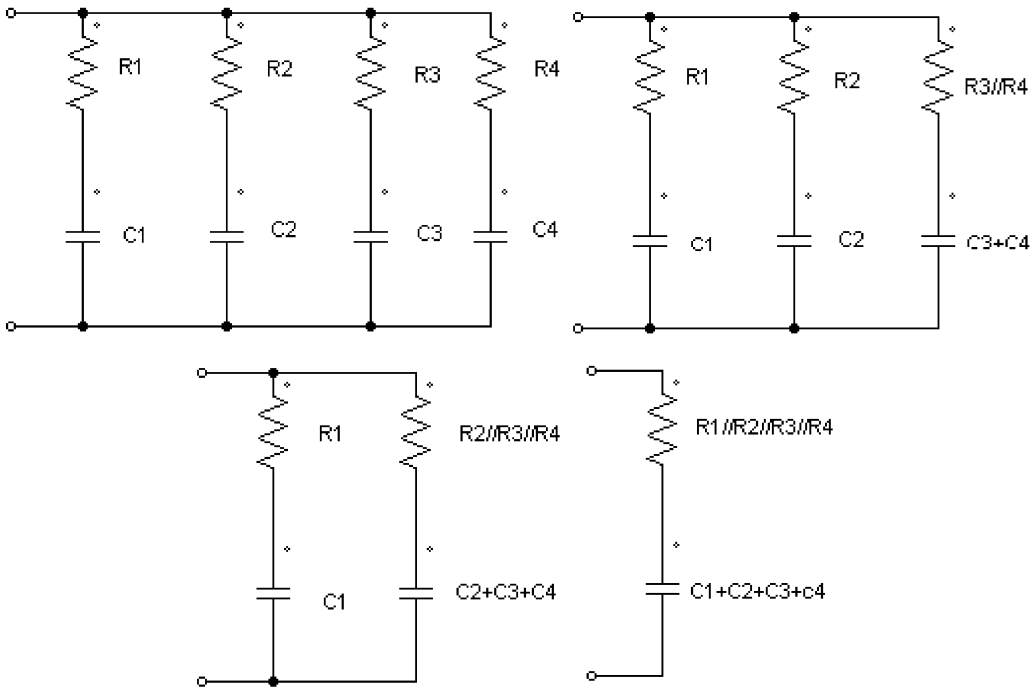

Figure 15: Order reduction of the supercapacitor parallel RC equivalent model [27]

A similar model of the supercapacitor has been derived by some researchers. It is similar to the RC parallel brunch model as the three separate branches are characterized by different time constants [28]. The fast branch is responsible for the short time total resistance and capacitance, while the rest describe the charge redistribution of supercapacitor in longer times. The redistribution of charge can account for the temporary decrease in supercapacitor voltage immediately after charging, as well as the temporary increase in supercapacitor voltage immediately after discharging as shown in Figure 13.

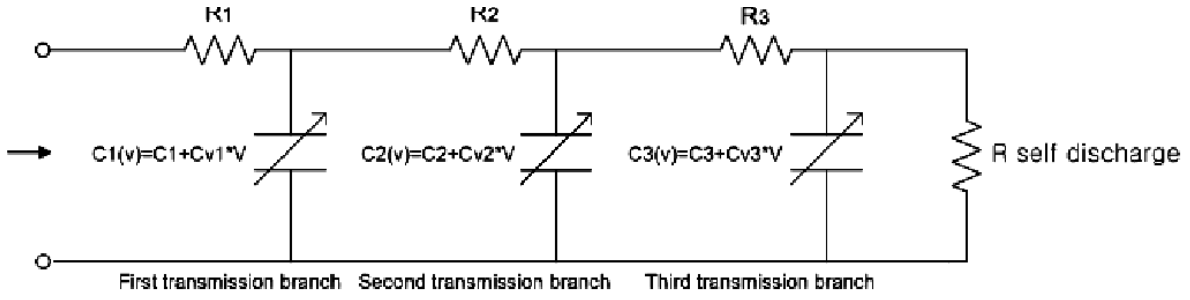

Figure 16: Equivalent model of the supercapacitor with three different time constant capacitors [28]

Figure 17 illustrates that this model correspond closely to the experimental data of a Maxwell's Boostcap supercapacitor. This method of modeling requires the measuring of voltage deviation during discharging of the supercapacitor to achieve an accurate model.

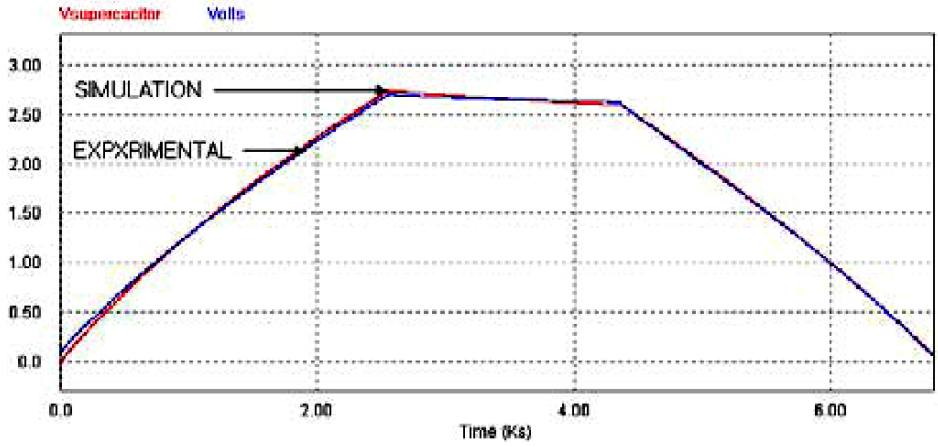

Figure 17: Charge and discharge of the Maxwell Boostcap 3000F at 3A constant current [28]

Some researchers had carried out experiment to determine the series inductance of the supercapacitor. This data is not released by any supercapacitor manufacturer. Thus, this value has to be determined experimentally. To do so, the test circuit has to be optimized so that the circuit inductance is minimized. A capacitor of known value is then inserted, from which observing voltage and current oscillation due to resonance, the inductance can be calculated [29]. The equivalent model of the supercapacitor would be shown in Figure 18.

Supercapacitor inductance is known to be very small, in the range of nH. Therefore, the measured value can be easily influenced by external factors. While this method can possibly derive a better supercapacitor model, it is very tedious and suffers inaccuracy due to test circuit stray inductance. Models that include three RC branches can already model supercapacitor with great accuracy, thus further incorporation of inductance in modeling is questionable.

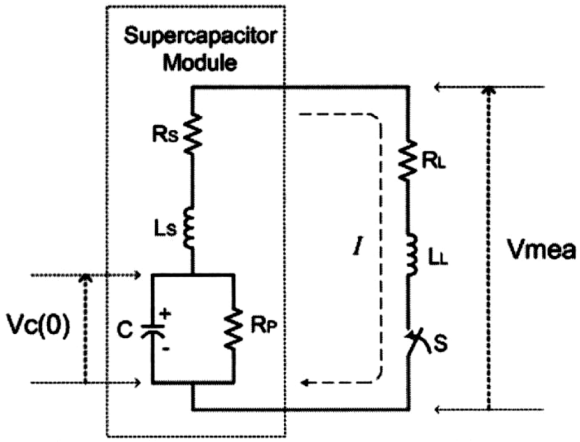

Figure 18: Equivalent circuit of supercapacitor during discharge [29]

It is a standard procedure to incorporate electrolytic capacitors at the input and output leg of SMPS in an attempt to smoothen the voltage and current waveforms. This results in a near DC voltage input/output with little AC fluctuation, as observed in Figure 19. As a result, it is not necessary to consider high frequency models where significant energy transfers occur due to the use of SMPS. In such an application, it is justified to use the corresponding low frequency ESR and capacitance.

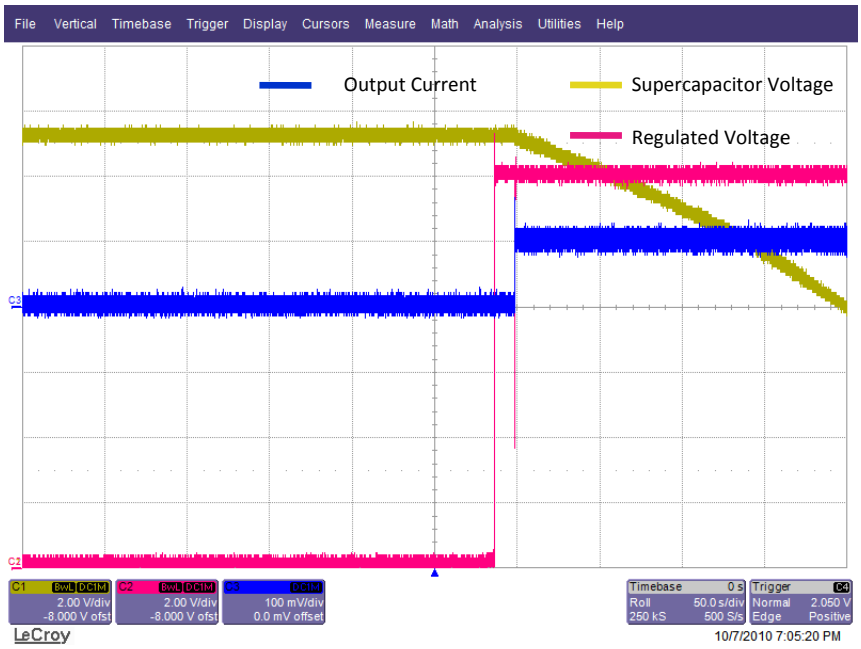

Figure 19: Voltage and current waveforms during SMPS operation

When considering the application of supercapacitor, the transient behavior of supercapacitor would arguably be of more importance when compared to the long term behavior which include relaxation and charge redistribution. The voltage regulator that works with the supercapacitor only sees the supercapacitor transient behavior during operation. It is only during the idle state that the supercapacitor experiences the charge redistribution phase. As such, it was justified to use a basic RC model with accurate DC ESR and capacitance accounting for changes in voltage. This makes supercapacitor modeling for the relevant application much easier.

3.5 Proposed Supercapacitor Model – The Modified RC Model

With justification that only the transient period is of concern to the voltage regulator, the supercapacitor model can be constructed using low frequency ESR and capacitance, taking into account the relevant parameter fluctuation with voltage, as observed in Figure 20.

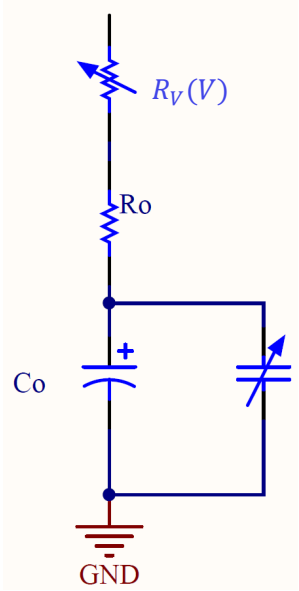

Figure 20: Modified basic RC model

Although the modified RC model is structurally similar to the basic RC model, it takes into account the capacitance fluctuation with voltage by the introduction of the term $K_V(V)$ as well as the term responsible for ESR fluctuation with voltage, $R_V(V)$. To construct the model, supercapacitor parameter fluctuation with voltage has to be known. Therefore, accurate supercapacitor parameters through reliable acquisition methods has be achieved, failure which is unable to accurately reflect the change of supercapacitor parameter with voltage.

3.6 Supercapacitor Parameter Acquisition

To accurately model the supercapacitor, reliable and accurate parameters has to be acquired. In addition, it is also known that supercapacitor parameters can provide useful State of Health (SOH) information. As supercapacitor ages, the capacitance decreases while the ESR increases. When the ESR has increased to 100% or that the capacitance is reduced by 20%, the supercapacitor is deemed to have reached the end of its lifespan. Should the parameters be reliably obtained, reliable state of health information could easily be achieved as well.

The supercapacitor practical parameters are important in the building up of the electrical model. However, many standards exist even in the measurement of supercapacitor parameters, such as the International Electrotechnical Commission (IEC) 62391. The United States Advanced Battery Consortium (USABC) test manual is a complete set of test procedures specifying a series of constant current and power test to characterize the supercapacitors. The 5C discharge rate is utilized for the characterization tests, which indicates the constant current value corresponding to discharging the supercapacitor from V_{max} to V_{Min} in a 12 minute discharge [30].

From the USABC test manual, it is unable to provide a distinctive method to measure the ESR of the supercapacitor. However, it is generally agreed that the ESR could be denoted as

$$ESR = \frac{\Delta V}{\Delta I}. \quad (3)$$

The discrepancy in ESR measurement data is generally be due to ΔV. ΔV can be obtained from several methods which would be listed below:

1) ΔV is the voltage drop at the onset of a constant current step.
2) ΔV is the voltage difference during the constant current step and 5 seconds after the current step was removed.
3) ΔV is the voltage difference between the idle state and the extrapolation of Supercapacitor linear voltage drop (due to constant current step) back to 0 in the time domain.
4) $\Delta \tilde{V}$ is the sinusoidal voltage injection from the EIS.

The ΔV values do fluctuate according to different methods. In addition, it is also believed that ESR vary with current and voltage conditions. Therefore, several standards had been published in order to provide a platform for comparison and evaluation.

The supercapacitor ESR has several importance to the application of itself: The ESR determines the power capability of the supercapacitor. Increment of ESR will result in lower power capability.

For a constant current discharge, the voltage of the capacitor becomes

$$V_{O,d} = V_O - I_d R_{ESR} \quad . \quad (4)$$

Therefore, the output power would be denoted by

$$P_d = I_d V_o - I_d^2 R_{ESR} \quad . \qquad (5)$$

When maximum power is delivered,

$$\frac{dP_d}{dI_d} = 0 = V_O - 2I_d R_{ESR} \quad , \qquad (6)$$

the maximum current, $I_{d,Max}$ is:

$$I_{d,Max} = \frac{V_O}{2R_{ESR}} \, , \qquad (7)$$

and the maximum power, $P_{d,max}$ is denoted by

$$P_{d,Max} = \frac{V_O^2}{4R_{ESR}} \, . \qquad (8)$$

Equation (8) shows that doubling the ESR value results in the reduction 50%, for the maximum current and a reduction of 75% in the maximum power deliverable. As such, small deviation in ESR can result in a large impact in power and current ratings. It also implies that the supercapacitor maximum power and current ratings are dependent on the usage frequency. Therefore, it further highlights the importance of knowing the supercapacitor parameter.

3.7 AC Parameter Measurement

The most popular method of measuring supercapacitor ESR includes the use of EIS. The test procedures for supercapacitor usually involve operating the EIS in frequency sweep mode at varying voltage states from 0.01Hz to 1 KHz. The EIS is often tuned to apply small voltage ripple amplitude of 10mV superimposed to a DC offset equivalent to the supercapacitor

terminal voltage. This method is highly automated and conducive as connection of the supercapacitor to the EIS is all that is required.

From Figure 11, it can be found that the capacitance of supercapacitor vary according to frequency. Therefore to achieve cross comparison, one had to determine the frequency in which voltage measurement was done. Consortiums such as USABC recommend 1 KHz as the frequency standard. Generally, the capacitance and ESR at 1 KHz would be approximately half that of 0.1Hz. As 1 KHz was unlikely to be the operating frequency of any supercapacitor, it was neither reasonable to determine supercapacitor parameter at that frequency nor to use values that were derived from that frequency.

3.8 Using Voltage Recovery Method to Measure ESR

This method considers the recovery of supercapacitor voltage after the discharge current has been removed. As observed in Figure 21, the recovered voltage is observed to be V_r. While this method has the merit of no capacitance influence when the discharge current is removed (I=0), one has to consider both the charge equalization in the supercapacitor itself as well as the supercapacitor self discharge phenomenon. This placed an uncertainty on the settling time for voltage measurement after the current pulse is removed. The longer the settling time, the more prone the supercapacitor is likely to suffer from the self discharge phenomenon. Short settling time can result in insufficient voltage recovery.

Thus, it is difficult to place a standard measurement procedure on this method across different supercapacitors, as different supercapacitors of different ratings are likely to have different optimal settling time. In actual experimentation, 5 seconds is too short to see full voltage recovery. During initial stages of experiment, it is noted that the recovery can take

tens of minutes to stabilize. This is crucial as every milli-Volt of V_r can cause a small deviation in the already small ESR.

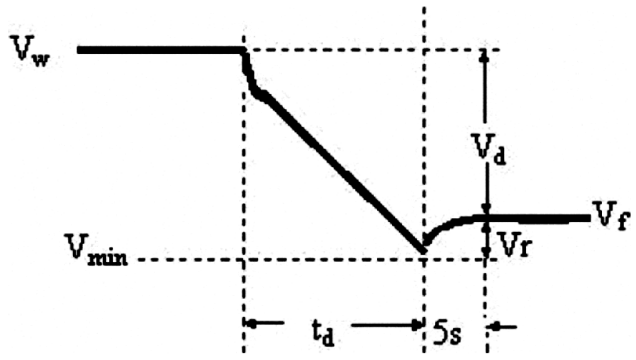

Figure 21: Theoretical waveform for constant current discharge followed by relaxation

3.9 Using Instantaneous Voltage Drop Method to Measure ESR

This is a relatively simple method involving the detection of instantaneous voltage rise/drop due to the ESR upon the onset of a charge/discharge process. When the current pulse is known, the ESR is known as:

$$\boldsymbol{R_{IR}} = \frac{\Delta \boldsymbol{V}}{\Delta \boldsymbol{I}}, \tag{9}$$

where $\Delta V$is the instantaneous voltage drop and I is the current at that instant time, as shown as V_1 in Figure 22. This method does not take into account the voltage drop due to the capacitance of the device. The merit of this method is that due to the instantaneous voltage acquisition, voltage drop due to capacitance effect can be ignored.

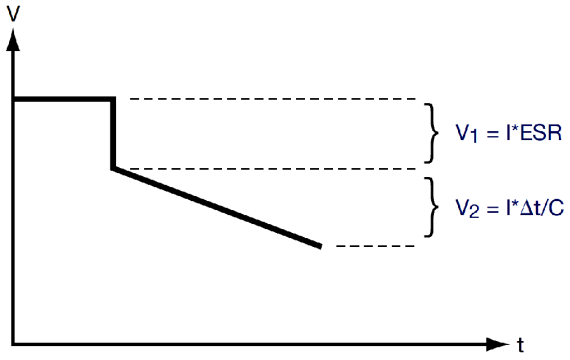

Figure 22: Instantaneous voltage drop due to current draw [31]

In fact, this method is so simple that many manufacturers like AVX adopted it to identify their ESR value [31]. Other manufacturers like Cap-XX consider ΔV to be the voltage drop after a current step was applied for 50µseconds [32].

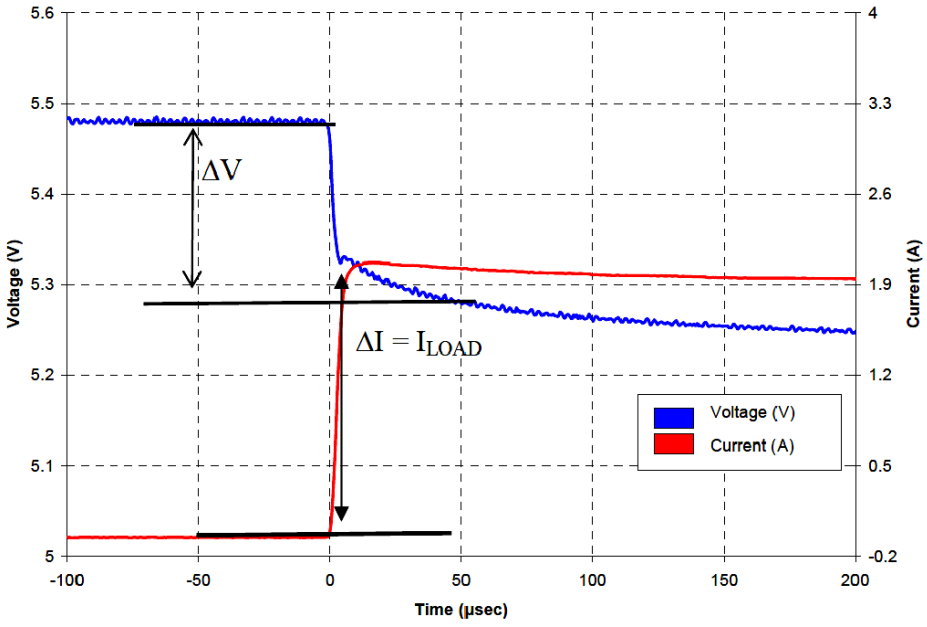

Figure 23: AVX method of measuring ΔV 50µseconds after a step current pulse is applied [32]

Figure 23 shows the supercapacitor voltage at the first 200µseconds upon the application of a current pulse. It is noted that the supercapacitor voltage dropped sharply upon the initiation of current draw, and it gradually flattened out to experience a linear voltage drop. It can cause

confusion and uncertainty as to when to acquire the voltage drop ΔV as the behaviour of different supercapacitor differs.

3.10 Using Constant Current Pulse Method to Measure ESR

This method is extensively used to determine ESR in battery testers involve the application of short current pulse of typically 3-10 seconds. The current pulse has to be constant in nature, and can be either charging or discharging. Theoretically, the supercapacitor experienced a linear voltage drop under a linear current draw, as stated by the principle of capacitor:

$$I_C = C\frac{dV_C}{dt}\ , \tag{10}$$

where I_C denotes the capacitor current, V_C the capacitor voltage and C is the capacitance of the device. It is noted that the supercapacitor undergoes a linear voltage drop with a constant current pulse via:

$$\Delta V_C = \frac{-I_C}{C}\bullet\Delta t \quad . \tag{11}$$

However, it is also noted that on the onset of voltage drop, the capacitor voltage do not fall linearly, as seen in Figure 23. It is particularly evident in the first 50μSeconds of the initiation of current draw.

The constant current pulse method take into account the non-linear portion of voltage drop at the onset of constant current, by discarding that portion and instead extrapolating the linear portion backwards, as observed in Figure 24. The voltage value of the extrapolated linear portion at the instant the current pulse is applied would be termed V_{SS}. The difference between the initial voltage V_O and V_{SS} is known as ΔU. Therefore, the DC ESR R_{DC} is denoted by

$$R_{DC} = \frac{V_o - V_{ss}}{I} = \frac{\Delta U}{I} \quad , \tag{12}$$

where I is the amplitude of the current pulse.

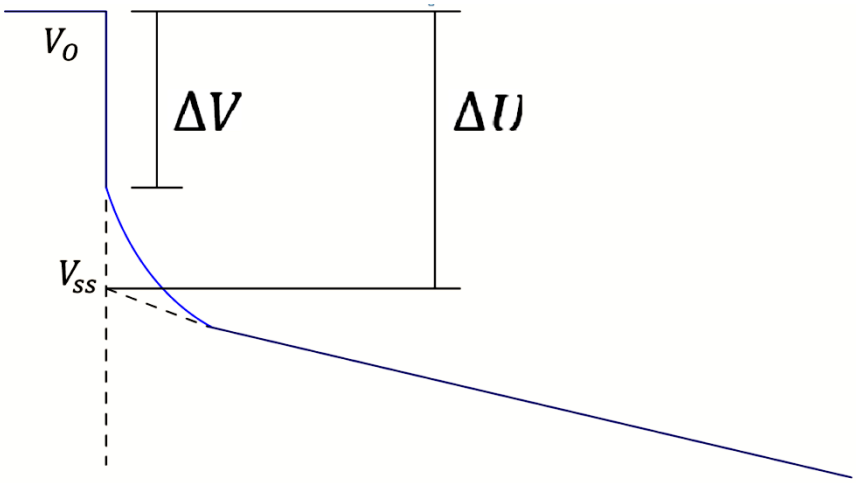

Figure 24: Constant current pulse method

3.11 Using AC Parameter Measurements to Measure ESR

A highly versatile RC measurement system which is capable of operating from 1 mHz to 1 MHz, whilst capturing data such as resistance, impedance, capacitance and phase angle at different voltage ratings was built. Customizable settings include amplitude of voltage ripple, frequency range, number of steps in the frequency range as well as the number of averaging attempts. This RC measurement system was fully developed from scratch.

This system incorporated a PXI-6133 Data Acquisition (DAQ) card, a pair of PXI-5406 Function generator, both from National Instruments (NI), as well as the power amplifier A01. The PXI-6133 card is a 14bit DAQ card capable of operating up to 300 MHz, which more than suffice where sampling rate is concerned.

The power driver A01 from DSI is a power amplifier capable of operating up to 1MHz in constant voltage mode with minimal distortions. It also has reasonably high current drivability of 5A. Its operating voltage was in the range of ±12V, compared to the supercapacitor maximum voltage of 2.7V, making it the ideal device for driving the excitation signal. It is capable of producing highly accurate and reliable current signal output. While the power driver is able to operate in both constant voltage and current mode, only the constant voltage mode was used in the experiment. The current mode suffers from periodic instability whilst driving the supercapacitor, namely due to optimization of the current mode to drive inductive devices.

During operation, one of the function generators was used to provide a DC offset while the other to provide the AC excitation signal. The DC offset indicates the target DC voltage the supercapacitor is to be tested at, while the AC excitation signal amplitude and frequency indicate the AC test conditions. The system's Graphic User Interface (GUI) allows the user to determine the DC offset and AC parameters independently, as observed in Figure 25.

The AC parameters include the excitation signal amplitude, frequency range, linear/log stepping and number of cycles to average in a frequency. As the signal from the function generator do not have sufficient drivability, the A01 was used to provide electrical drivability. Figure 26 illustrates the system flowchart of the RC measurement system while Figure 27 shows the experimental setup.

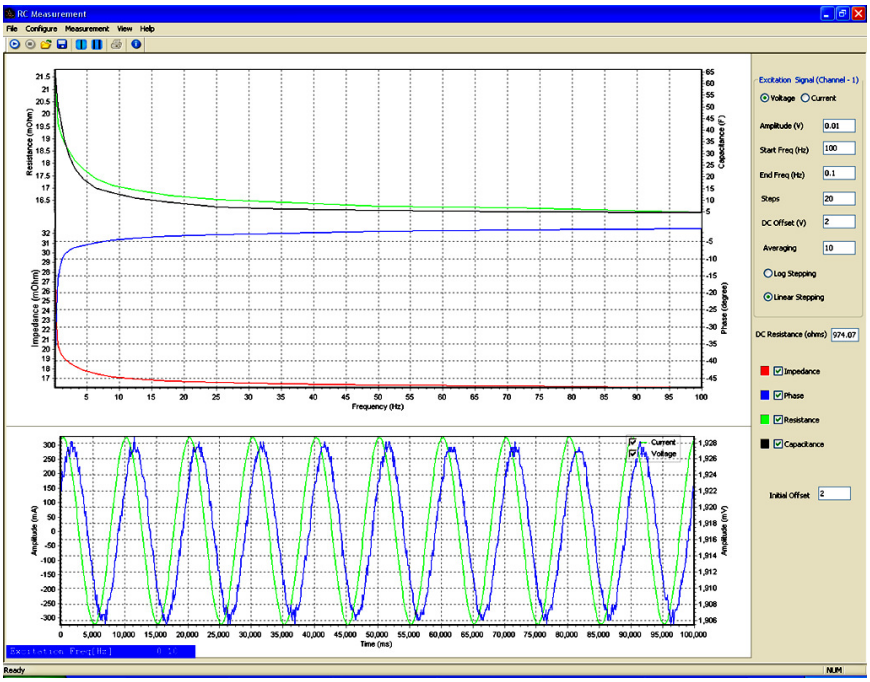

Figure 25: Control panel of the RC measurement system

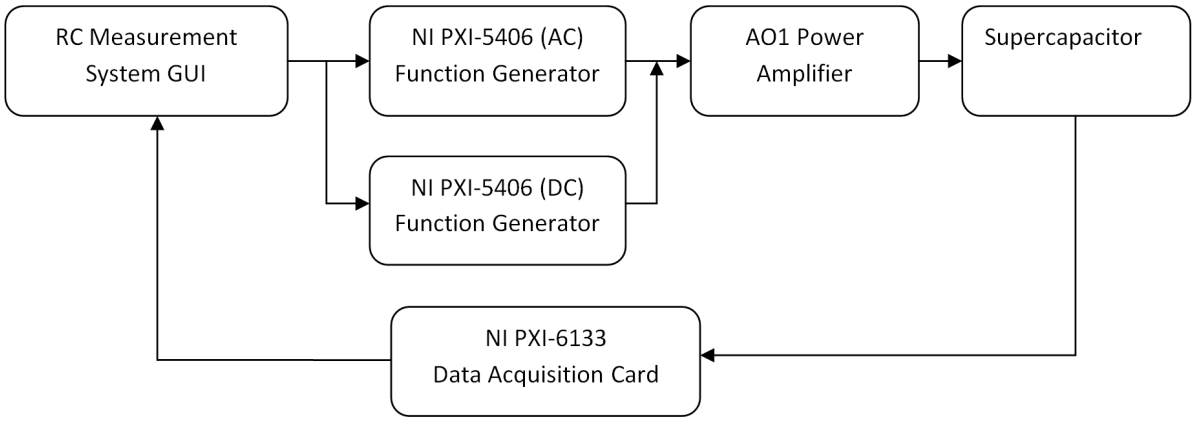

Figure 26: System flow chart of RC measurement system

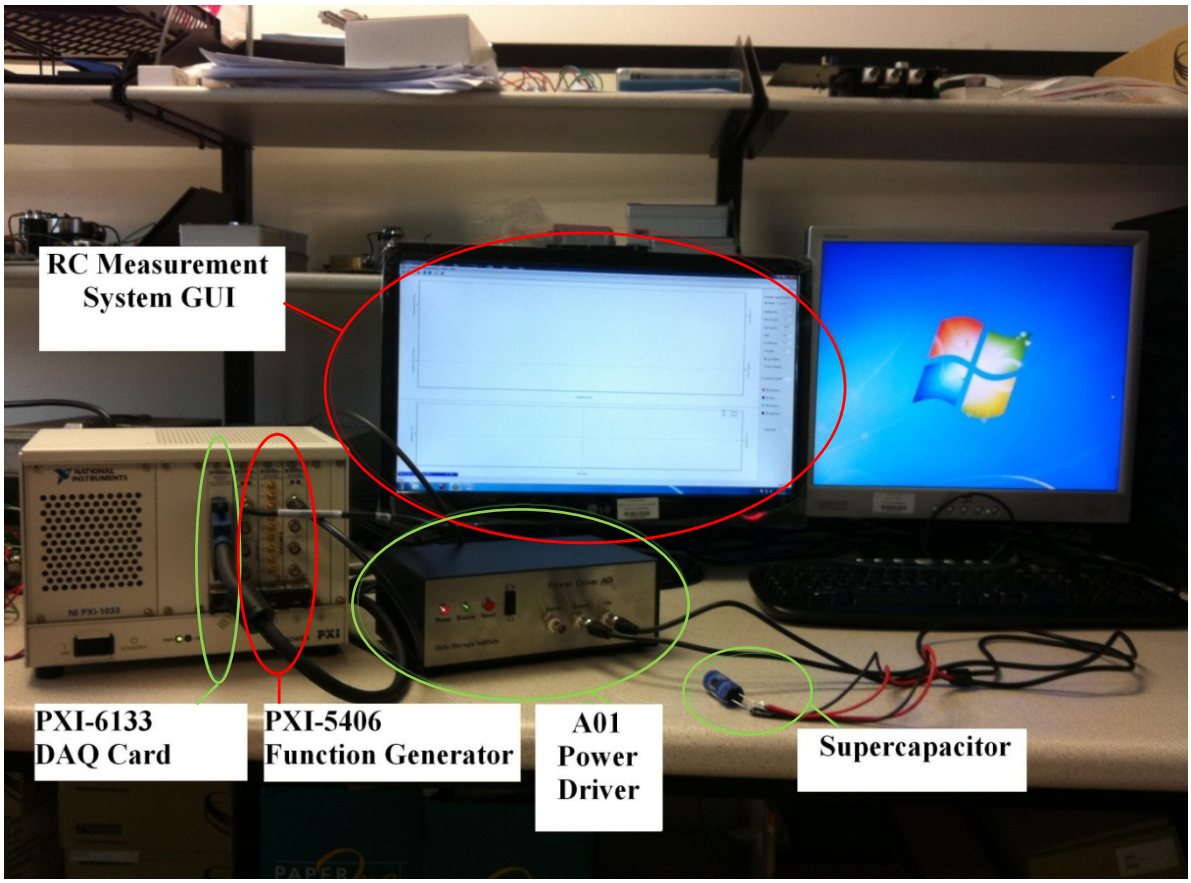

Figure 27: Experimental setup of RC measurement system

On triggering the software, each NI function generator produces a separate DC and AC excitation signal to A01 power driver operating in constant voltage mode. After which, the power driver replicates the sum of both signal in the form of voltage signal to the supercapacitor. At the lead terminal of the supercapacitor, the voltage signal is feedback to the DAQ card, together with the current signal obtained directly from the power driver.

The signals are analysed by performing a Discrete Fourier Transform (DFT). Discarding other frequencies, only the frequency corresponding to the excitation frequency is utilized. The excitation frequency is known as it is generated by the RC measurement software. When both the driving voltage and current amplitude are known, the impedance Z can be denoted by:

$$Z = \frac{\tilde{V}_{AC}}{\tilde{I}_{AC}} \ . \tag{13}$$

The phase delay, $\boldsymbol{\delta}$ between the function generator excitation signal and driving signal at supercapacitor terminals is used to calculate the phase difference ∅.

$$\varnothing = \delta \times f \times 360^{\circ} \quad . \tag{14}$$

The inductance of Supercapacitor is known to be a very small value, typically in the range of nH. It is insignificant as compared to the capacitance and therefore reasonable to ignore it.

The capacitance, C, can be denoted by

$$C = \frac{Z \sin \varnothing}{2\pi f} \quad , \tag{15}$$

and the ESR, R_{ESR}, can be denoted by

$$\tilde{R}_{ESR} = Z \cos \varnothing \, . \tag{16}$$

Figure 28 shows a diagram demonstrating the voltage and current waveform during parameter acquisitions.

The RC measurement system is able to obtain the supercapacitor ESR reading of a specified terminal voltage through a user defined frequency range. The experiment is repeated for the three supercapacitor specimens.

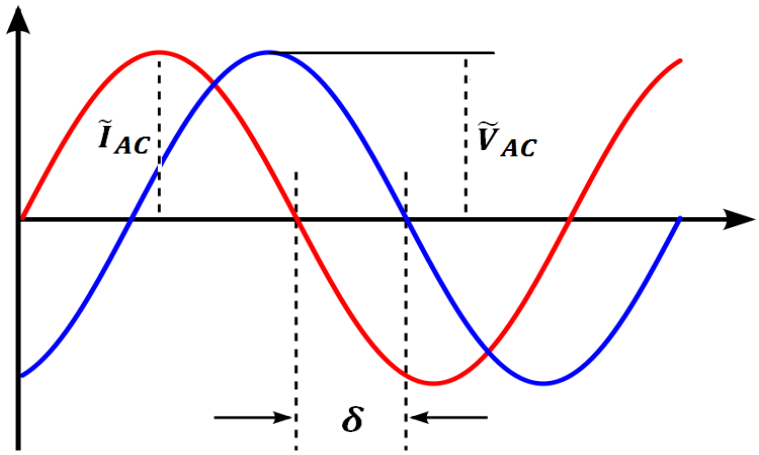

Figure 28: Diagram of AC excitation voltage and current waveforms with phase delay

To obtain the AC ESR through various voltages, the supercapacitor was initially fully discharged. The DC offset voltage was then set to command the system to charge the supercapacitor to the DC offset voltage. After stabilizing the voltage for approximately 30minutes, the AC excitation process began. Upon completion of the frequency sweep process, the results were saved for tabulation. The DC offset voltage was then manually increased through the software panel in intervals of 0.1V and the whole process was repeated.

Capacitance/ ESR/ Impedance/ Phase Vs frequency curve across different voltages were obtained through this RC measurement system at various voltages in frequency range of 0.1Hz to 100Hz and were tabulated in Figure 29 and Figure 30. The system was only made to operate up to 100Hz as it was unlikely for any supercapacitor application to operate beyond 100Hz.

The results obtained are in sync with most other researchers: The higher the frequency, the lower the capacitance and ESR/Impedance. Figure 29 shows that the supercapacitor capacitance decreased by as much as a factor of 10 under operation at 100Hz when compared to that at 0.1Hz. That immediately implies that the supercapacitor is not suitable as a high

frequency energy buffer device. Data from all three supercapacitors indicate that the capacitance variation at low frequency is large while the difference is much smaller at higher frequencies.

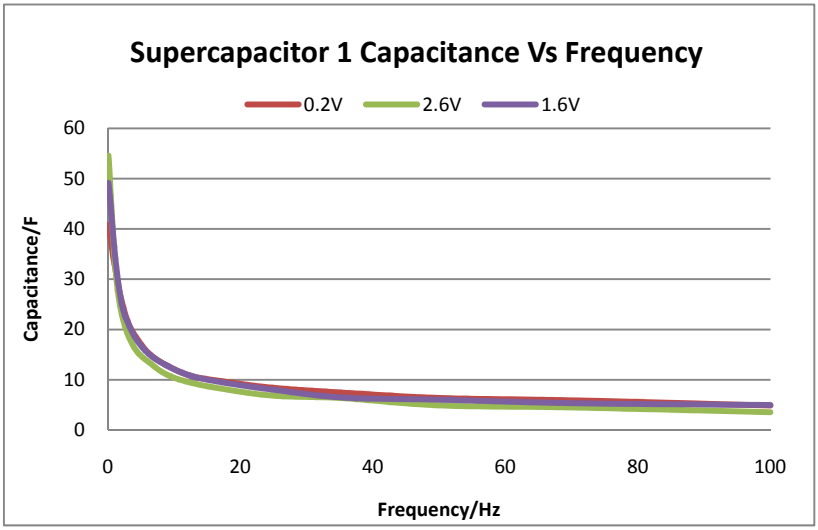

Figure 29: Supercapacitor 1 capacitance VS frequency sweep curve

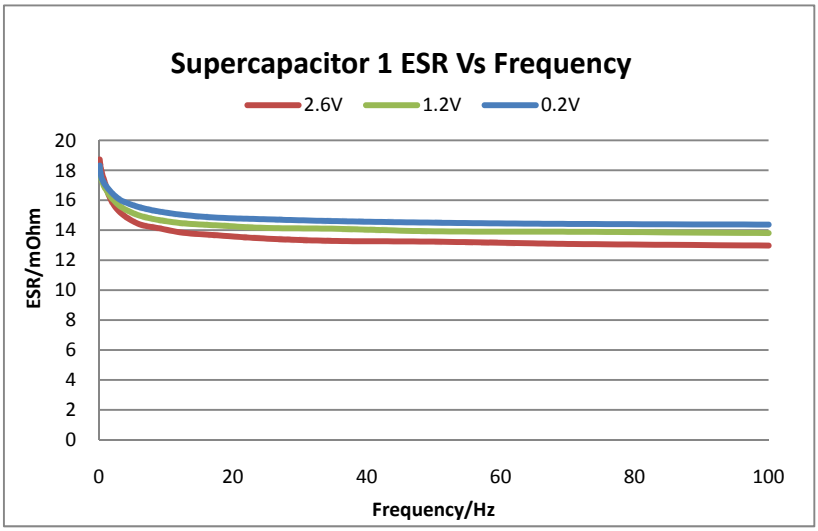

Figure 30: Supercapacitor 1 capacitance VS frequency sweep curve

All 3 supercapacitors suffer ESR drop at high frequencies, but supercapacitor 1 exhibit an interesting trend: The higher the voltage, the higher the low frequency ESR, but the high

frequency ESR was lower as compared to a lower voltage state. There is a cross over point in which the ESR of lower voltage state eventually became higher than the higher voltage state as frequency increases. This trend is visible in Figure 30 and the effect summarised in Figure 31. Figure 32 and Figure 33 shows the supercapacitor 2 and supercapacitor 3 ESR variation with voltage respectively, which is indicative of common EDLC behaviour.

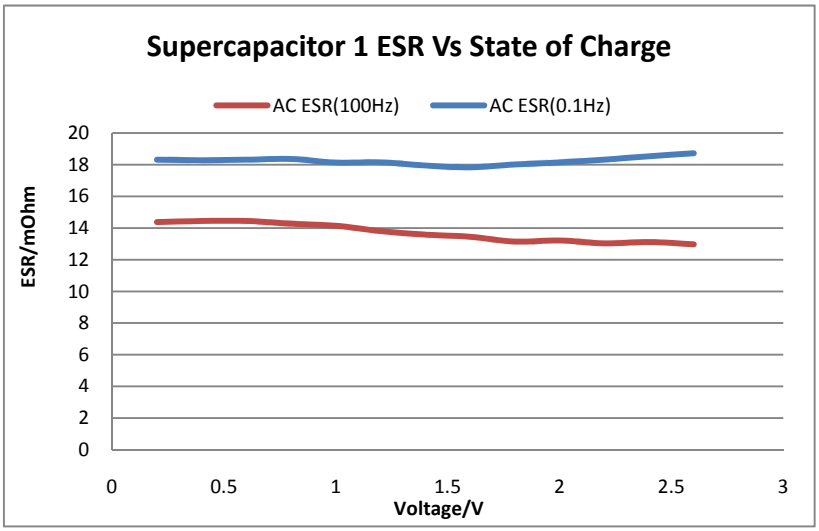

Figure 31: Supercapacitor 1 ESR Vs state of charge at 100Hz and 0.1Hz

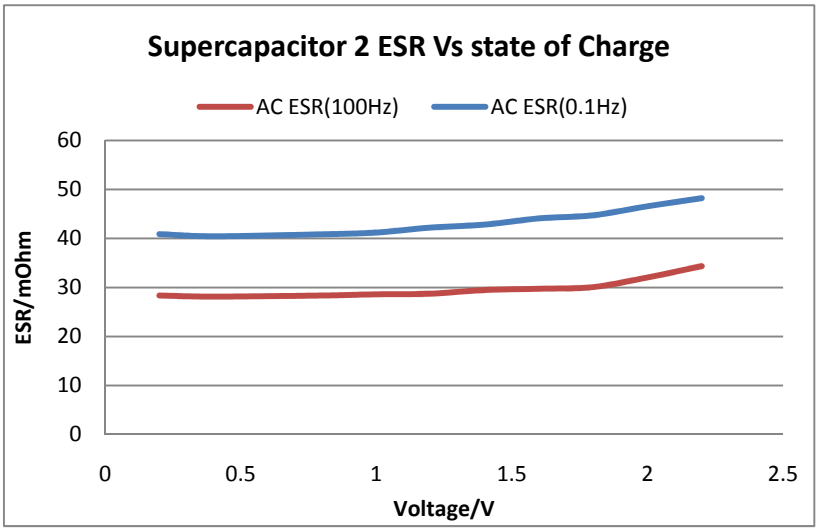

Figure 32: Supercapacitor 2 ESR Vs state of charge at 100Hz and 0.1Hz

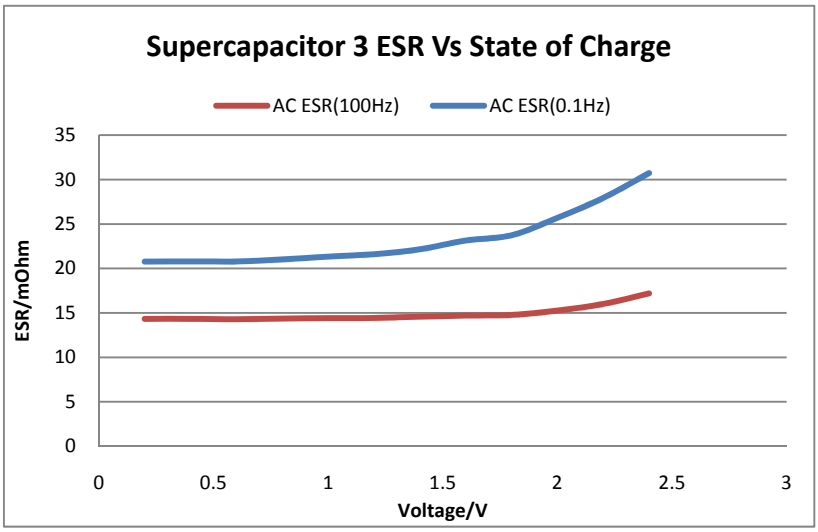

Figure 33: Supercapacitor 3 ESR Vs state of charge at 100Hz and 0.1Hz

3.12 IR Drop Measurement Procedure

The IR drop method was setup according to the schematic as seen in Figure 34. The NI PXI-6133 DAQ card was used to read the voltage across the supercapacitor terminals. Voltage difference across the sampling resistor was acquired via the PXI-6133 as well. Doing so, it could translate to current flowing through the circuitry through:

$$I_{circuit} = \frac{V_{Diff}}{R_{Sampling}} \quad . \tag{17}$$

The DC power supply was used to provide a DC bias so that the current drawn throughout the experiment was approximately constant across different supercapacitor voltage states. To minimize the voltage drop effect due to capacitance, two reasonably large power resistors of 10Ohm each were connected to the circuit in series so as to limit the current drawn to approximately 0.3A. That is, $V_{DC} + V_{SC} \approx 6V$. Where V_{SC} indicate the supercapacitor voltage while V_{DC} indicate the DC voltage bias due to the DC power supply.

Maintaining this relationship, the current drawn during this period remained unchanged. A square pulse of 1Hz was then applied to the MOSFET to initiate the IR drop so that the instantaneous voltage drop could be registered. Due to the small current drawn in each pulse, the supercapacitor voltage remained largely consistent before and after the current pulse. This way, one could be sure that the voltage drop due to capacitance is minimal and that the voltage drop was mainly due to the ESR.

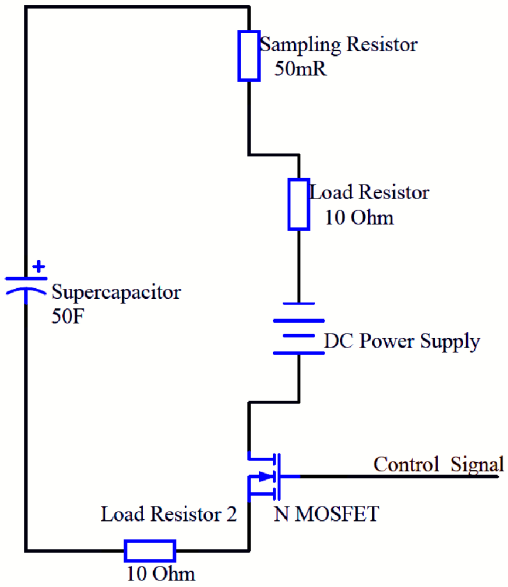

Figure 34: Schematic of IR drop measurement method

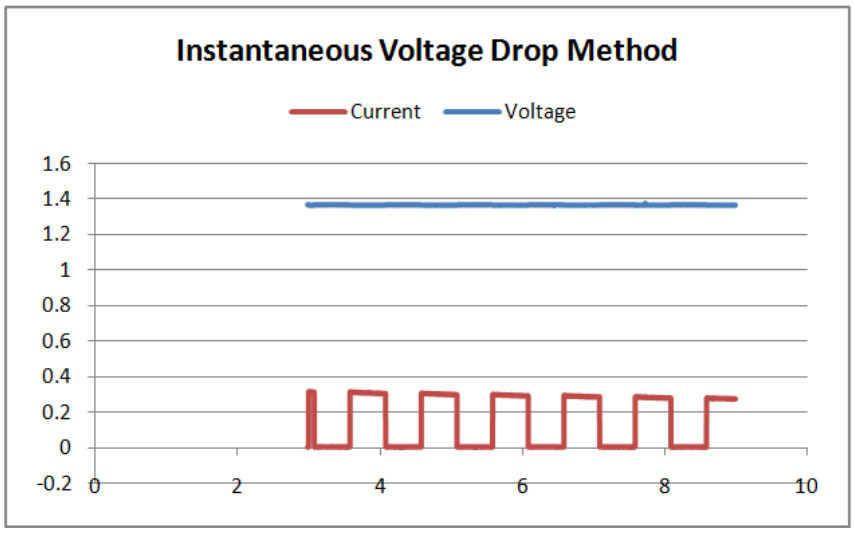

Figure 35: Instantaneous voltage drop method

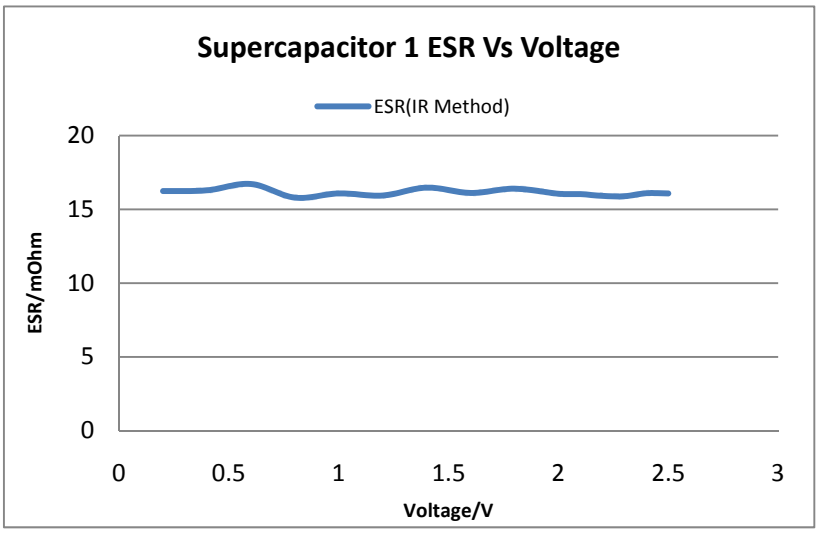

Figure 36: ESR of supercapacitor 1 using instantaneous voltage drop method

Figure 36 shows that the ESR of supercapacitor 1 is approximately constant throughout the operating voltage from 0.2V to 2.7V using the IR method. It was desirable to increase the magnitude of current pulse so that the voltage drop could be more prominent, yet doing so brought about the voltage drop due to the capacitance effect. A voltage drop of approximately 10mV was measured for a current pulse of 0.6A in this experiment. Noise influence on readings of this level is tremendous. An average of 20 results on the same run was calculated for each voltage value.

3.13 Constant Current Pulse Measurement Procedure

Figure 37 illustrates the schematic of the constant current pulse measurement method. The IT8514C from ITECH was used as the programmable electronic load while the NI DAQ Card NI-6251 was responsible for recording the supercapacitor terminal voltage as well as the current pulse via the sampling resistor. Current pulse of 1A, 3A, 5A and 7A were used in the experiment, mainly due to the supercapacitor current rating limitations. In order to ensure a

constant current load upon turning on the MOSFET, the programmable electronic load was set to run before the control signal was applied to turn on the MOSFET. The schematic and operation description of the MOSFET module is discussed in Appendix C.

Upon initiation of experiment from the host PC, the NI-6251 sent the control signal to the MOSFET module to start the constant current pulse operation. The card began the data acquisition simultaneously. Due to the high sampling rate used, the data was stored in binary format which was later analysed using MATLAB software. Figure 38 shows the experimental setup of the constant pulse system while Figure 39 shows such an experiment attempt.

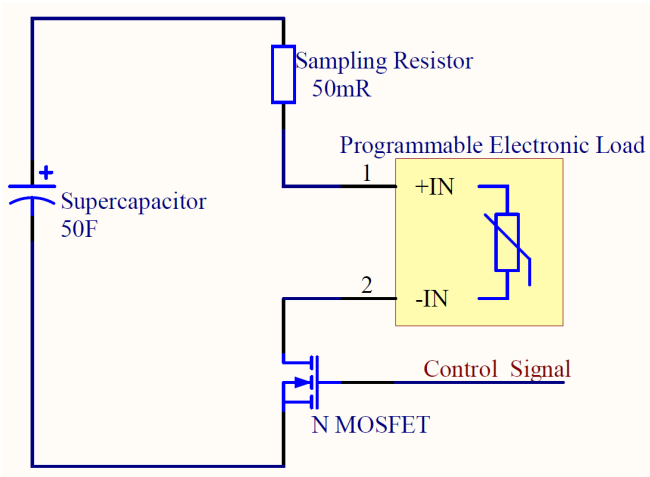

Figure 37: Schematic of current pulse measurement method

Figure 39 shows the voltage state of Supercapacitor 1 at constant current discharge of 7A. At the onset of current draw, the initial voltage drop does not show a linear voltage drop. It took approximately 0.2 seconds before the curve gradually straightens to a steady state linear voltage drop. It is clear that taking the slope of initial voltage drop would give rise to erroneous results. Therefore, the steady state voltage drop ΔU should be the difference between the initial voltage state and the Y-axis intercept of the gradient due to the linear voltage drop.

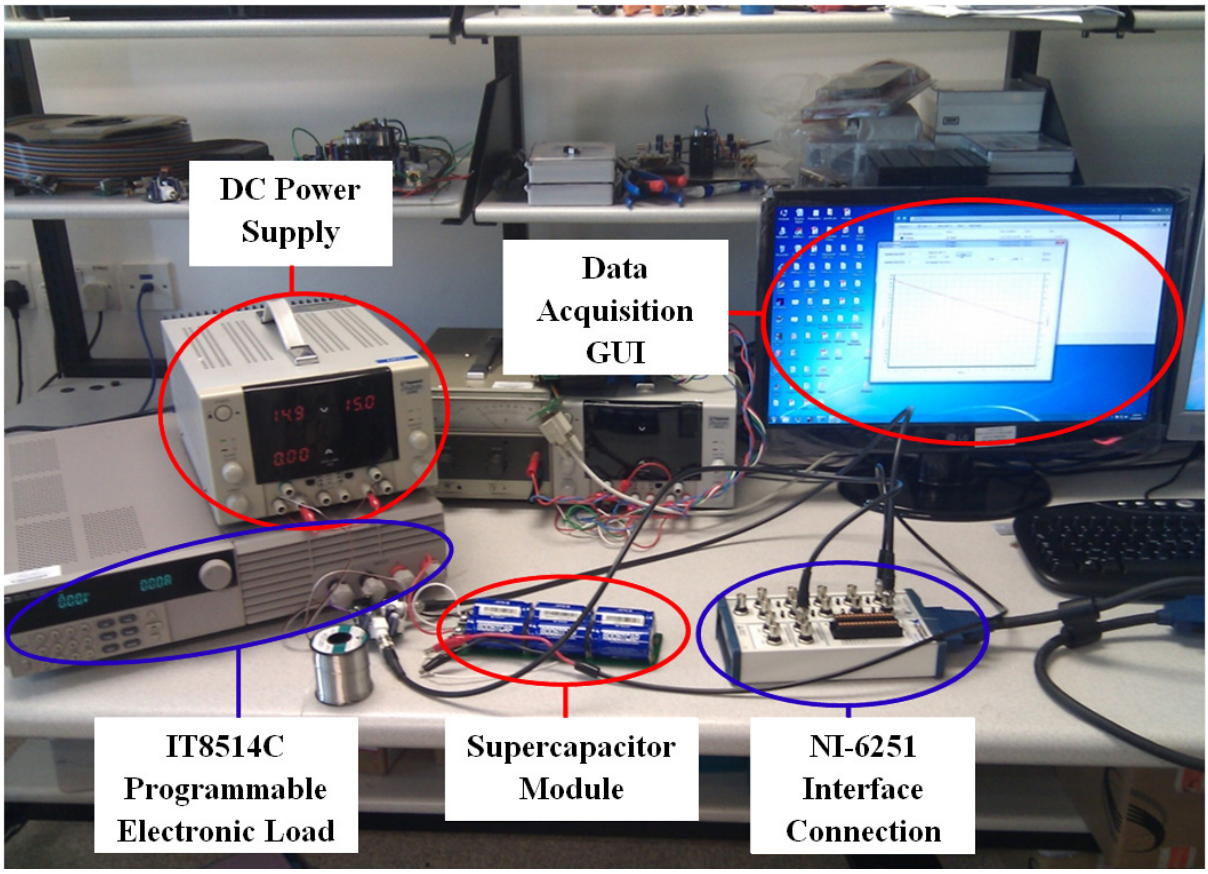

Figure 38: Experimental setup of the DC ESR measurement system

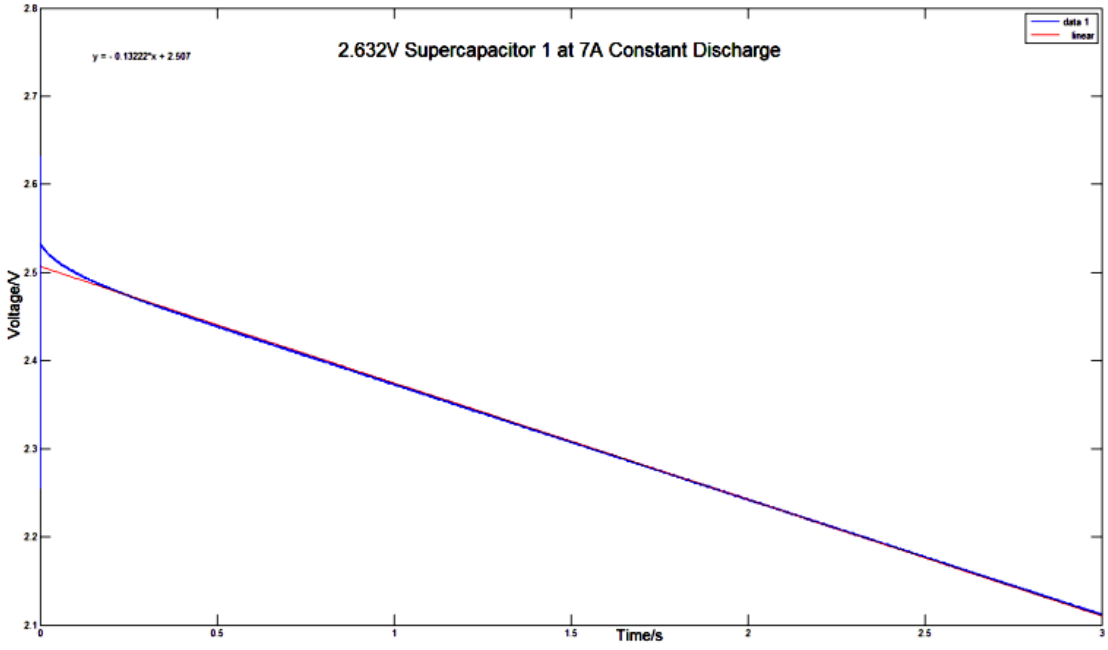

Figure 39: Constant current discharge profile of supercapacitor 1

As a result, a current pulse sufficiently long for the voltage curve to straighten is necessary before (12) can be applied to obtain the DC ESR. Using any gradient point before the voltage curve straightens is likely to produce ESR values several times smaller than that of the DC ESR value. This DC ESR is of particular importance as it coincides with most supercapacitor applications: Most supercapacitors are required to charge/discharge for several seconds in the least. Therefore, this DC ESR is particularly suitable for consideration in practical systems.

For ensure consistency, all gradients are taken at 1.5 seconds upon the start of the discharge process, where the voltage drop is largely linear. The results are tabulated in Figure 40-42, with direct comparison to AC ESR. It is noted that the DC ESR generally increases with increasing supercapacitor voltage, but is lower than AC ESR at 0.1Hz for all cases.

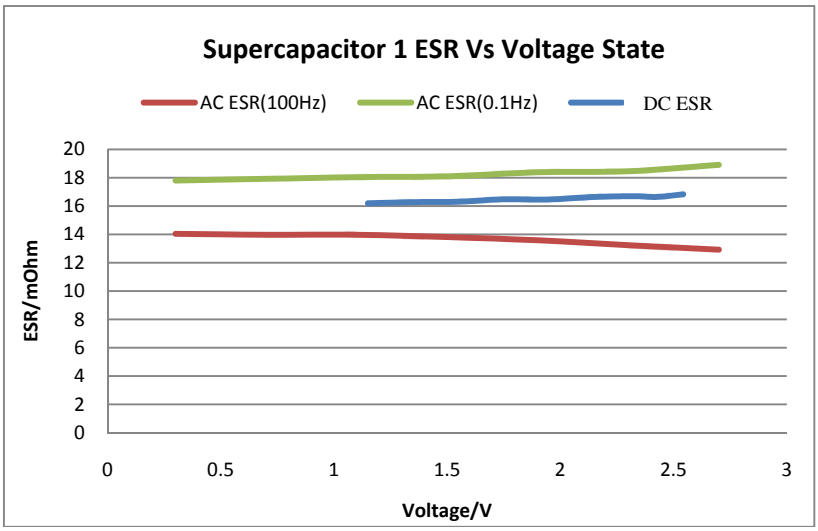

Figure 40: Supercapacitor 1 ESR comparison

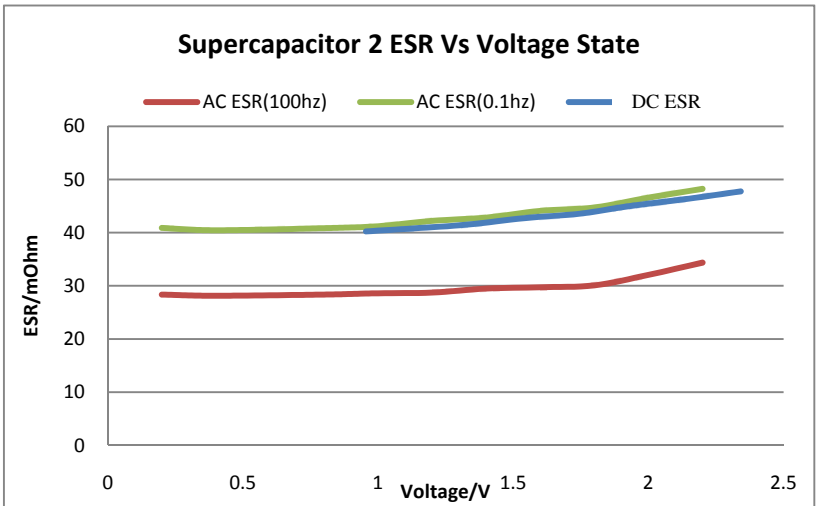

Figure 41: Supercapacitor 2 ESR comparison

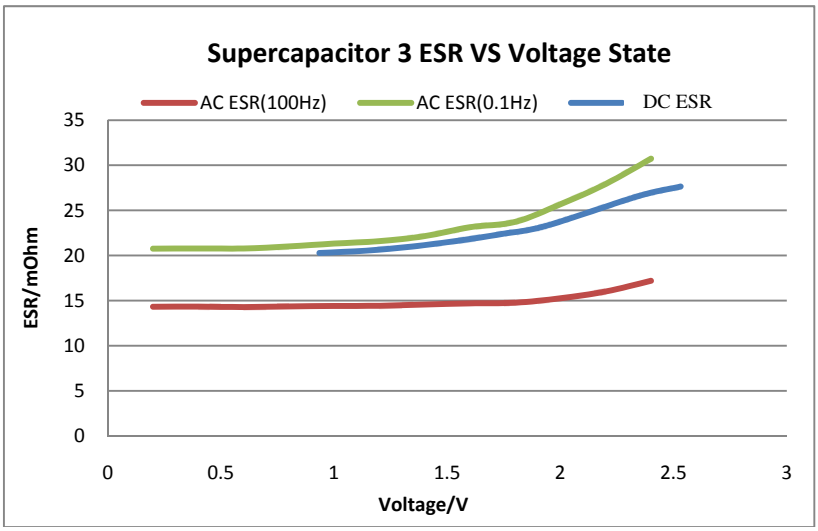

Figure 42: Supercapacitor 3 ESR comparison

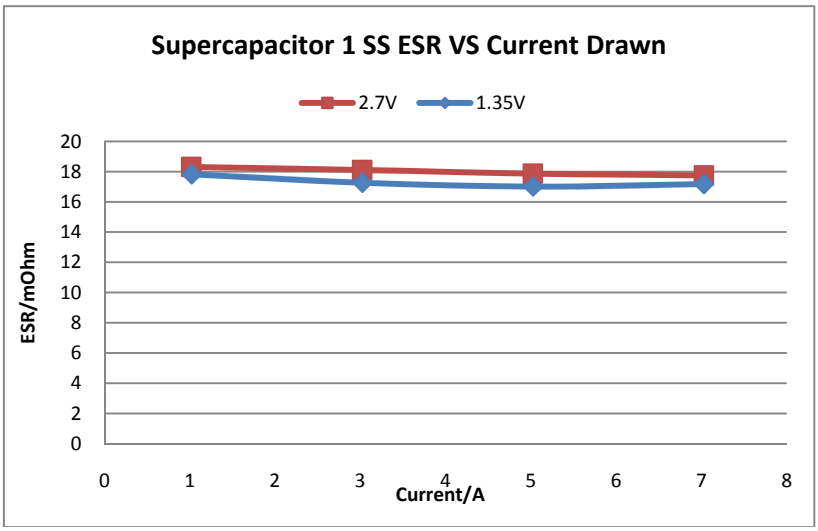

Figure 43: Supercapacitor 1 DC ESR Vs current

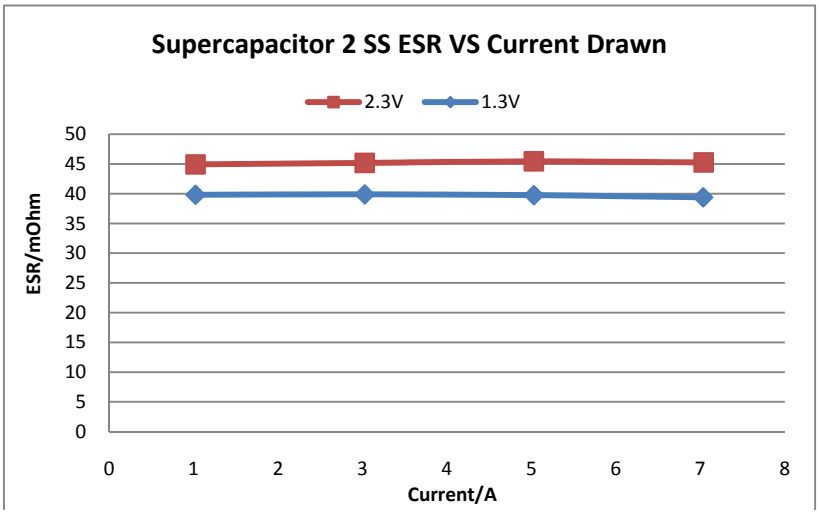

Figure 44: Supercapacitor DC ESR Vs current

Figure 43 and Figure 44 indicate that the DC ESR is generally constant when the supercapacitor is subjected to different current operation. There is however, a very slight decrease in ESR at higher current conditions. The DC ESR variation with voltage is far more significant than that of current. Therefore, it can be concluded that current conditions has little or negligible effect on the ESR readings.

Of particular interest is the slope of the linear voltage drop. The supposedly linear portion of the voltage curve suffers a slight change in gradient, which affects the ΔU value. This ultimately impacts the DC ESR results. Therefore, it is possible to observe the ESR change in the time scale, also which can be converted to the frequency scale for comparison with the AC ESR.

As the current pulse is only responsible for discharging, it is deemed to be equivalent to the half-period of an AC cycle where the supercapacitor discharges. Therefore by doubling the time interval in which the gradient is obtained, one can compare the AC ESR at the same frequency as the DC ESR. Table IV shows the changes in ESR and ΔU as a result of gradient taken at different time intervals.

Table IV: Supercapacitor 3 voltage slope variation under constant current

Time Interval	Frequency	Gradient	ΔU	ESR/mOhm
1.5	0.333333	0.13266	0.1848	26.389
2	0.25	0.12723	0.1929	27.547
2.5	0.2	0.12374	0.1998	28.531
3	0.166667	0.12123	0.2061	29.435
3.5	0.142857	0.11955	0.2111	30.149
4	0.125	0.1182	0.2158	30.822
4.5	0.111111	0.11706	0.2203	31.469
5	0.1	0.11593	0.2253	32.177

The results tabulated by both AC and DC ESR as shown in Figure 45 are very similar and shares the same trend. The difference between both ESR at any one frequency is 1 mΩ at maximum. This indicates that the AC ESR is as reliable as the DC ESR at low frequencies.

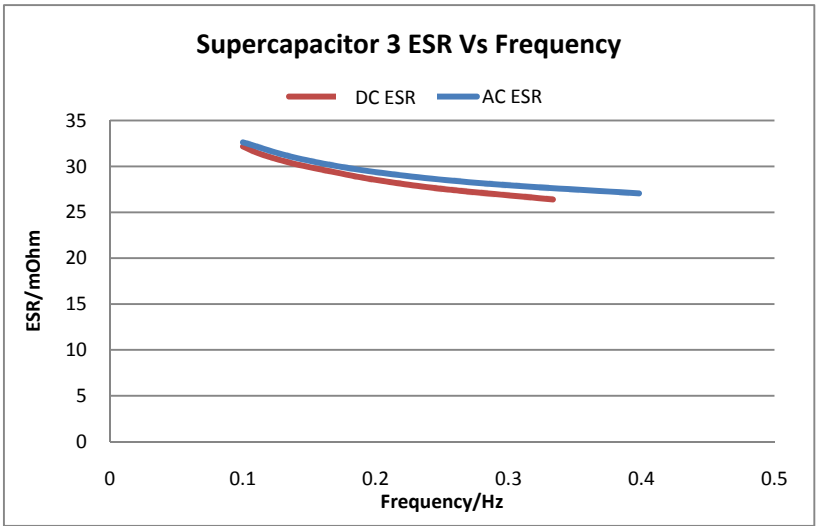

Figure 45: Comparison of DC ESR and AC ESR in frequency domain

3.14 Implications of Measurement Results

It is to be noted that both the IR drop method and constant current pulse measurement methods are vastly similar in principle. The only difference lies in the ΔV and ΔU used for the voltage drop. As such, it is reasonable to deduce that the IR drop method is a special

condition of the constant current pulse method without taking the initial non-linear voltage drop into consideration. Through experiments with very low current conditions to minimize error due to the capacitance effect, the IR drop method still yielded ESR values smaller that of the constant current pulse method.

This can be explained whilst considering that at the onset of current draw, the voltage drop is not linear, as experienced by the constant current pulse measurement method. Therefore, the ΔV is likely to be smaller than ΔU at the same current conditions. This would cause the IR drop method to arrive at an ESR smaller that of the DC ESR. In fact, this method measures the smallest DC ESR value. One can also view the non-linear portion of the constant current pulse measurement method to equate to ESR in the higher frequencies.

Based on the practical data acquisition, the supercapacitor is not suited for high frequency applications. The storage capability can decrease by a factor of 10 or more at a mere 100Hz, negating the advantages of the supercapacitor energy density. In fact at higher frequencies, electrolytic capacitors become a potential candidate.

To harness supercapacitor maximum energy capacity, complete charge/discharge typically takes tens of seconds at the maximum current rating. A current-mode bidirectional SMPS is usually employed to monitor the charging/discharging process so as to ensure that the supercapacitor module is operating under rated current conditions. This ultimately increases the reliability of the supercapacitor module besides catering it to individual applications. Under constant current charge or discharge situations, the SMPS can monitor the supercapacitor module ESR through the constant current pulse method. Typically, supercapacitor applications require the supercapacitor to sustain charge or discharge in the

range of a few seconds in the least. Therefore, the SOH function can be integrated into the SMPS with high accuracy using the constant current pulse method.

Test conditions aside, both the USABC and IEC 62391 standards demand ESR to be calculated through the IR drop method. Whilst the test conditions are stringent and following which replication of results is undoubtable, calculation of supercapacitor ESR through the IR drop method is likely to deliver a smaller ESR value non-indicative of real life operational situations. As a matter of fact, the IR drop method measures the highest frequency DC ESR.

Upon acquiring the supercapacitor parameters relations with regards to frequency, voltage and current conditions, one can proceed to model the supercapacitor.

3.15 Dynamic Model of Supercapacitor

The BPAK0058 E015 B01 supercapacitor module from Maxwell has 6 supercapacitor each rated at 350F connected in series to construct a module rated at 58F and 15V. Using the AC RC measurement system, the supercapacitor parameters were acquired at 0.1Hz resulting in the ESR values between 20.267mΩ to 18.5mΩ. This is in line with the published ESR value of 19mΩ from the manufacturer datasheet. The capacitance is found to vary between 62.76F to 48F. Both the ESR and capacitance maximum value occurs when the terminal voltage is at the maximum voltage of 15V while the lowest value occurs when the terminal voltage is at the lowest value. The results are summarized in Figure 46 and Figure 47, and it was observed that the ESR and capacitance increases approximately linearly with supercapacitor voltage. The supercapacitor module is used in the experiments described in the thesis following on.

For a supercapacitor that exhibits linear capacitance gain with voltage, the supercapacitor capacitance and voltage is denoted by

$$C = C_O + K_V \bullet V_C \,, \tag{18}$$

where, C is the resultant capacitance, C_O the base capacitance value, K_V the capacitance gain per volt and V_C the supercapacitor voltage.

The Supercapacitor ESR and voltage relationship is denoted by

$$R = R_O + R_V \bullet V_C \,, \tag{19}$$

where, R denotes the resultant ESR, R_O the base ESR value and R_V the resistance gain per volt.

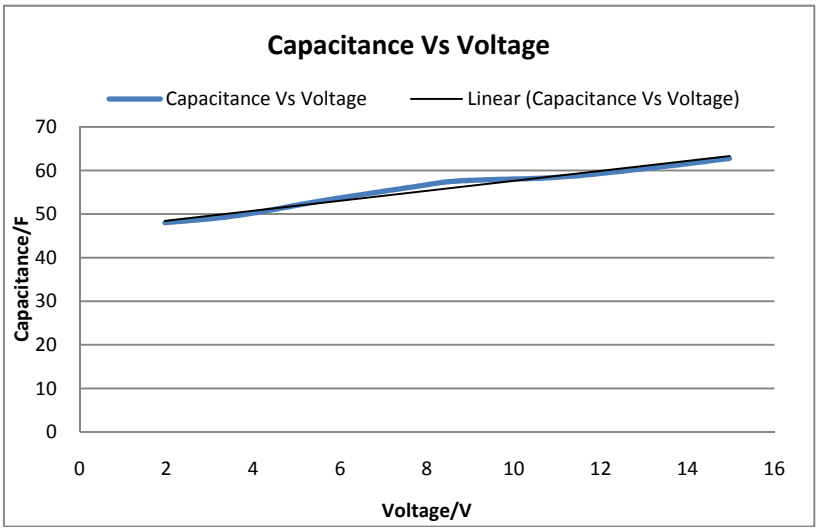

Figure 46: BPAK0058 E015 B01 Capacitance Vs Voltage curve

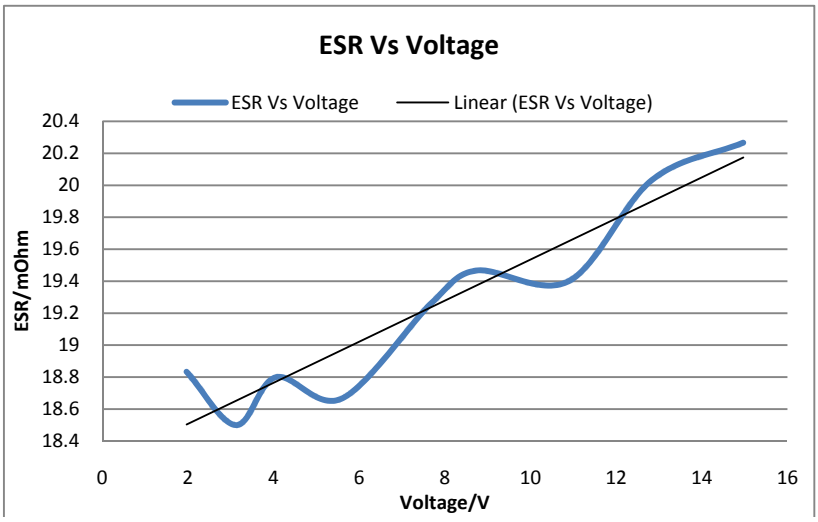

Figure 47: BPAK0058 E015 B01 ESR Vs Voltage curve

Using approximation algorithm, the curves in both Figure 46 and Figure 47 can be linearized.

The parameters of the line can be obtained as the ones shown in Table V:

Table V: Experimentally determined variables for BPAK0058 E015 B01

Parameters	C_O	K_V	R_O	R_V
Values	46.19 F	1.143 F/V	18.25 Ω	0.128 Ω /V

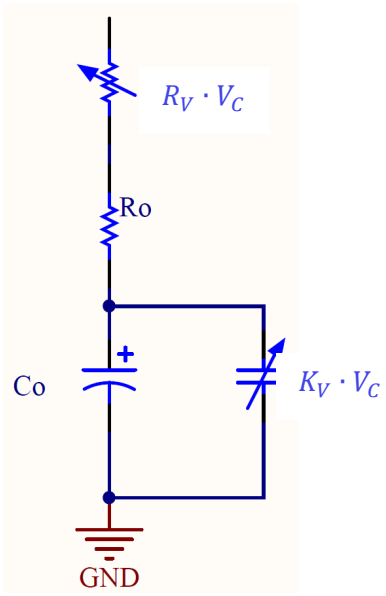

Figure 48: Modified single branch RC model with linear parameter increment with voltage

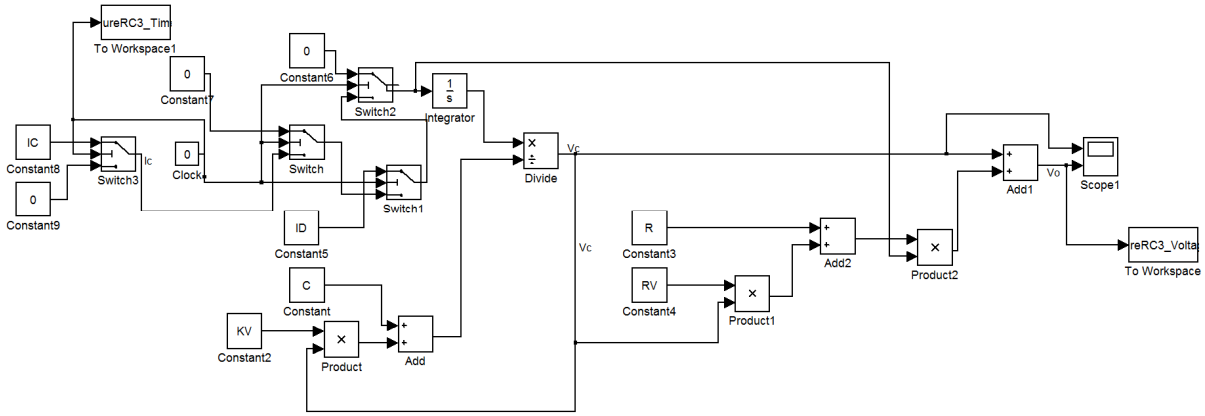

Figure 49: Modified single branch RC model - Simulation (SIMULINK) model

Figure 48 shows the modified single branch model, with the simulation model shown in Figure 49. This is to allow the single branch model to reflect the supercapacitor capacitance and ESR variation with voltage. Figure 50 shows the comparison of simulated results of the 15V supercapacitor module in comparison to the practical results.

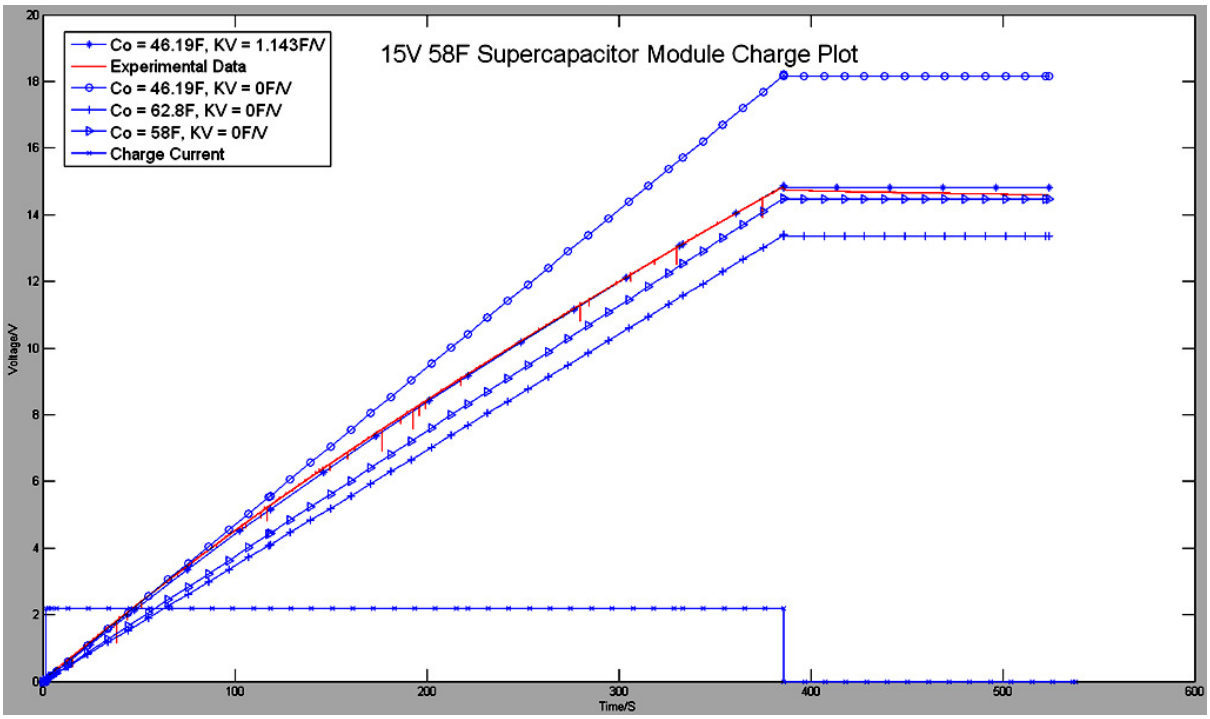

Figure 50: Simulation result comparison with variation in C_O and K_V

It is noted that inclusion of the K_V parameter allows the modified RC model to reflect the non-linear rise in terminal voltage under constant current conditions. Using both the minimum and maximum measured capacitance value without taking K_V into account gives severally different results. This is also the case when the published value of 58F is applied without taking K_V into consideration. Whilst the simulation model is unable to reflect the charge equalization effect, as observed during the period 386 – 524 seconds, the transient operation closely resembles the practical data.

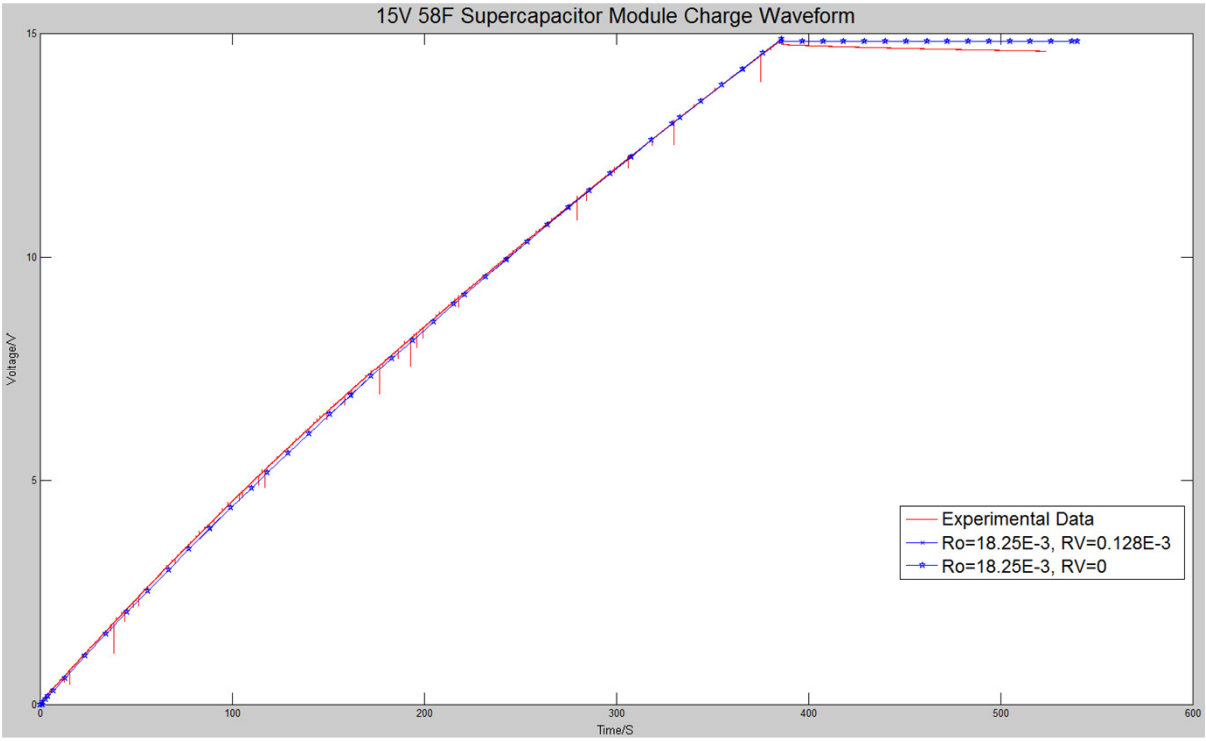

Figure 51: Basic RC model with variation with K_V

Figure 51 shows the simulated results with regards to the supercapacitor under constant current charge of 2.18A, with capacitance parameters fixed at $C_o = 46.19\,F$ and $K_V = 1.143\,F/V$ whilst varying R_V. It is noted that R_V has negligible effect to the simulation results. However, Figure 52 shows the significance of R_V, as it can cause degradation of

maximum power at the maximum voltage. Therefore, inclusion of R_V is necessary in the modified RC model as it helps determine the maximum power obtainable through the supercapacitor.

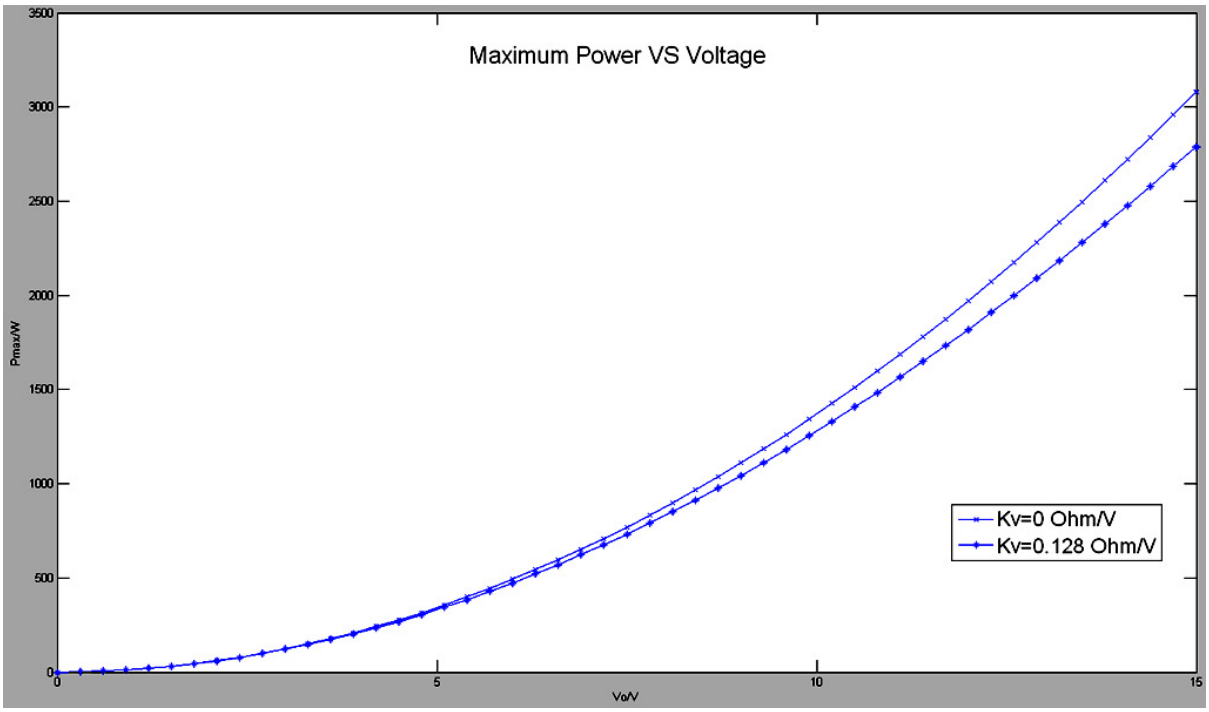

Figure 52: Maximum power Vs supercapacitor voltage

3.16 Chapter Conclusion

It was discussed that during the operation of supercapacitor, the parameters change due to transient voltage variation is generally more important than the long term relaxation process. Several supercapacitor models are proposed, amongst which the basic RC model is the simplest model but is unable to reflect charge equalization. The multiple branch models are able to include the charge equalization process but branch parameter calculation is a tedious and slow process. Furthermore, the relaxation process is not as crucial to supercapacitor operation as the fluctuation of low frequency ESR and capacitance is to changes in voltage.

Four supercapacitor ESR measurement methods for supercapacitor parameter measurement are analyzed and compared. It was pointed out that capacitance measurement is less of an issue compared to ESR measurement. Variation in capacitance value does not cause much impact in applications, whereas the ESR can affect much power capability by deviation in the range of a few mΩ. This is taking into consideration that supercapacitor ESR is generally very small.

Four methods were discussed for the acquisition of supercapacitor ESR. The voltage recovery method was determined to be unreliable due to parasitic effects such as charge equalization as well as leakage charge that can skew results. The instantaneous voltage drop method was discovered to be a subset of the constant current pulse method, which measures the highest frequency ESR of the later. Therefore, the ESR obtained through instantaneous voltage drop method was regarded as unreliable. It was experimentally determined that although the constant current pulse method was reliable and repeatable, the DC ESR acquired at different time of acquisition was different. It enabled the conversion of DC ESR to the frequency domain, which allowed it to be comparable to the AC ESR acquired using EIS. It was discovered that at the frequency domain, both the AC ESR and DC ESR are comparable and within a small tolerance, indicating that both methods were reliable in topology and results.

Several important results were discovered during experimentation, which include the variation of supercapacitor ESR and capacitance with voltage and frequency. Of interest was that the supercapacitor ESR does not vary significantly enough with current conditions to be taken into consideration for modeling. It resulted in a simpler supercapacitor model where parameters were independent of current.

It was also discussed that although several supercapacitor models are available today, the simple RC model was sufficient to model the supercapacitor when only the charge/discharge intervals are considered. This is due to the fact that although single branch RC model cannot simulate charge equalization, it is able to take into account the dynamic region during charge or discharge, which is only of importance to the SMPS operation. A Maxwell Supercapacitor module is experimented based on the understanding and the resultant parameters are obtained for model construction in the thesis. With the understanding of supercapacitor model and behavior, one can now consider the application of supercapacitor, in particular with the SMPS topology.

Chapter 4

Bidirectional SMPS Converters

4.1 Introduction

This chapter discusses and analyzes several bidirectional SMPS topologies for applying supercapacitor as an electric energy storage element. In chapter 2, several supercapacitor applications were mentioned. Some of the supercapacitor applications include operating it as an UPS energy storage device and/or a peak load shaving energy device. In particular, application of supercapacitor in EV is of much concern, although particularly difficult. During regenerative braking, the electric machine operates in the generator mode to convert the vehicle's kinetic energy into electrical energy. As the regenerated voltage was proportional to the vehicle speed, the generated voltage decreased with decreasing vehicular speed.

To effectively store the regenerated energy, the voltage regulator had to be able to charge the supercapacitor in a wide input voltage range. As the vehicle speed decreases due to regenerative braking, the regenerated energy caused the supercapacitor voltage to increase. The reverse is true as well: During vehicle move off, the supercapacitor discharge to assist acceleration. As the vehicle picks up speed, the load voltage required increases while the supercapacitor voltage falls. Therefore, this application necessitates the use of a voltage regulator that could handle the dynamics of both the input and output voltage changes. Through selection of regulators, the bidirectional hexa-mode buck-boost converter was

deemed uniquely suitable and was described and analyzed. The non-isolated bidirectional SMPS converter was chosen due to its ability to operate when the input voltage is higher or lower than the output voltage.

4.2 Classification of Voltage Regulator

Figure 53 shows a summary of popular regulator topologies. Switching regulators have inherently higher efficiency as compared to linear regulators, making them uniquely suited for energy transfer applications. The PWM regulator, commonly known as SMPS, is arguably the most popular switching regulator today, due to the high efficiency and wide number of topologies that allow it to be applied to countless applications.

All applications in chapter 2 are achieved with different types of SMPS. For either topology, a bidirectional SMPS is necessary and advantageous due to several reasons:

1) A bi-directional SMPS is able to control when to charge and the corresponding rate of charge. This is extremely important to supercapacitor as its ESR is extremely small and should there be no current regulation, most systems would suffer uncontrollable huge current draw.
2) Able to incorporate a wide range of operating conditions, including operating voltage range, current range and more.

Most Supercapacitor coupling SMPS are modified varients of the highly popular buck, boost, buck-boost, half bridge and full bridge converters. While most SMPS operates in uni-directional energy transfer, some topologies are capable of transferring energy bidirectionally.

Bidirectional SMPS has the ability to charge and discharge supercapacitor at any rate it is customized to, and is therefore considered the best candidate for supercapacitor application.

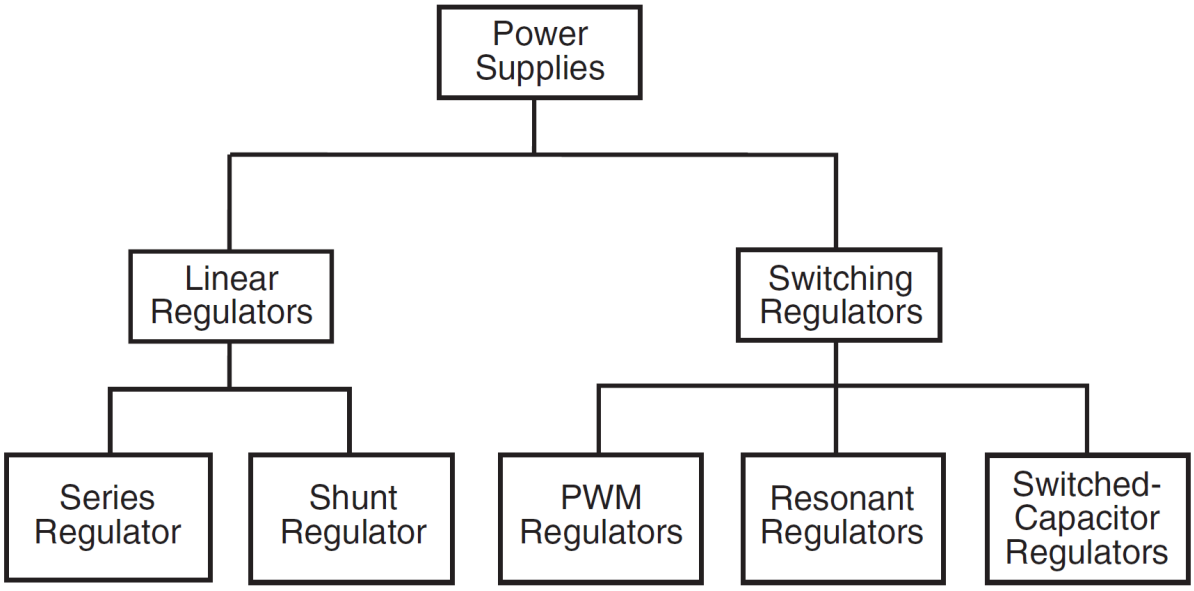

Figure 53: Summary of DC Regulators [33]

4.3 Bidirectional Buck-Boost Converter Topology

Figure 54 shows the simplified schematic of the bidirectional buck-boost converter. Unlike what the typical buck-boost converter, this design can only operate in the buck mode for the forward direction (charging supercapacitor), and boost mode for the reverse direction (discharge supercapacitor). The buck mode is achieved by controlling the switching of the IGBT T2, while operating T1 and T2 in complementary mode switching cycle results in a reverse directional boost converter. This SMPS is very popular and saw developments in many other organizations [12][14][34-35].

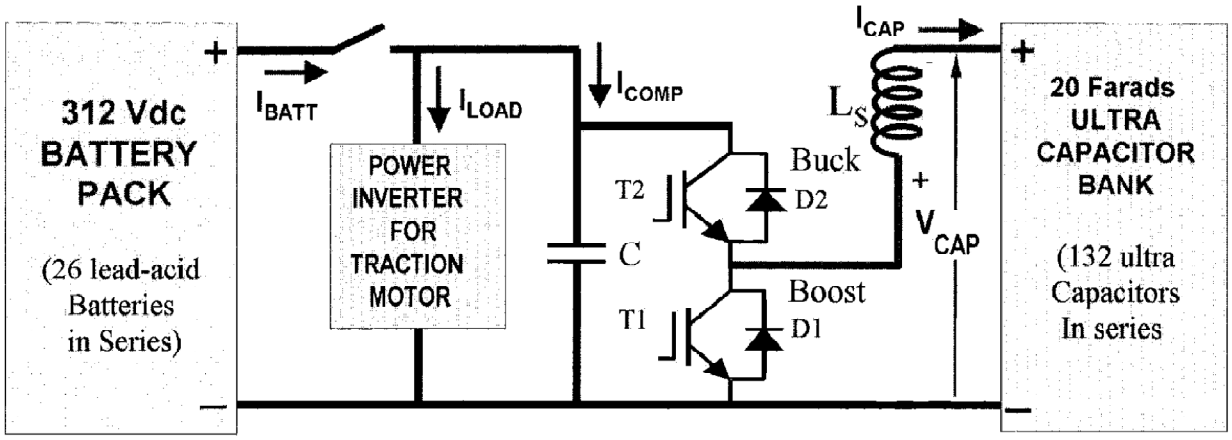

Figure 54: A typical modern supercapacitor system with bi-directional SMPS [12]

This system has the advantage of being able to transfer energy from the battery to the supercapacitor bank through the buck converter and supercapacitor bank back to the battery through the boost converter. In this way, energy can be transferred to the supercapacitor either from the battery during low load conditions or during regenerative braking. These stored energy can be used to charge the battery, or to be released for the next high power demand. This ensures that the battery maximum current is low while the Supercapacitor caters for the higher current demand, fulfilling the function of an active peak load shaving energy buffer.

This configuration has been very popular, especially when the battery and motor operating voltages are above that of the supercapacitor, mainly because the SMPS requires minimal components. The same SMPS schematic can be used in various ways. One method uses the supercapacitor as a backup energy buffer, which supplies energy to ensure consistent performance only when the battery is unable to produce the required energy [12]. Also, the Supercapacitor can be used to store the additional energy generated during regenerative braking after the battery has reached its capacity limits.

While there are many methods to effectively achieve active peak load shaving, some methods implements the hardware but do not realize the full potential of it. In particular, some researchers only use the supercapacitor as an energy backup [12]. Supercapacitors has the unique property of being able to charge and discharge at high efficiencies relative to batteries. In particular, no batteries to date are able to charge as rapidly as the supercapacitor. Standing from both the viewpoint of efficiency and performance, it is ideal to charge the supercapacitor module first, and upon reaching capacity limits, charge the battery.

Similarly, during discharging, it is more advantageous to utilize the supercapacitor first, followed by the battery. In addition, this can improve the battery life as it offloads most of the high power charging and discharging process to the supercapacitor, which has at least 2-3 folds more recharge cycles then the batteries. Thus, based on how one manages the supercapacitor system, efficiency and performance can differ even thought the same topology is used. This has serious implications as the same SMPS topology, has been widely implemented in other applications such as fuel cell systems, micro-grid systems and other Supercapacitor related systems.

Figure 55 shows the general block diagram of the most popular implementation of the supercapacitor in a HEV or PEV system. Figure 56 is but a version of what is shown in Figure 55 [36].

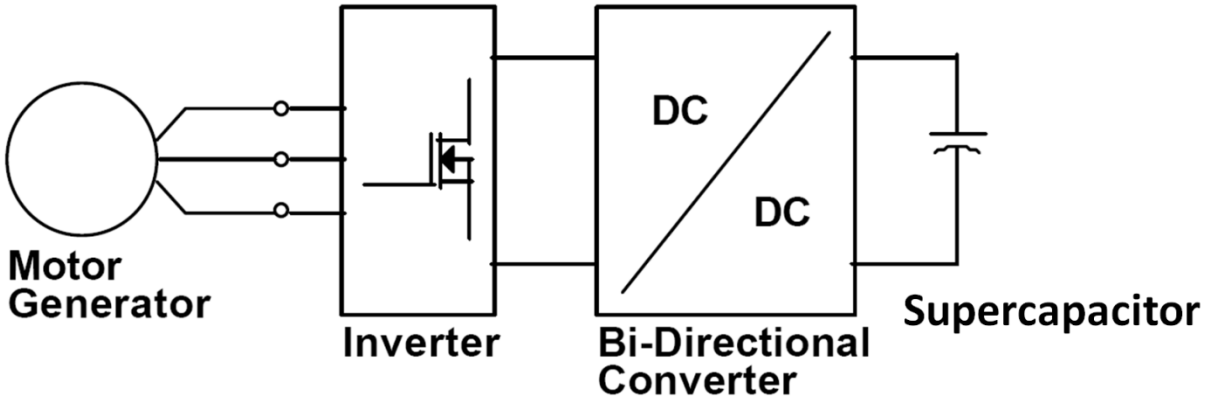

Figure 55: Supercapacitor system with SMPS Converter

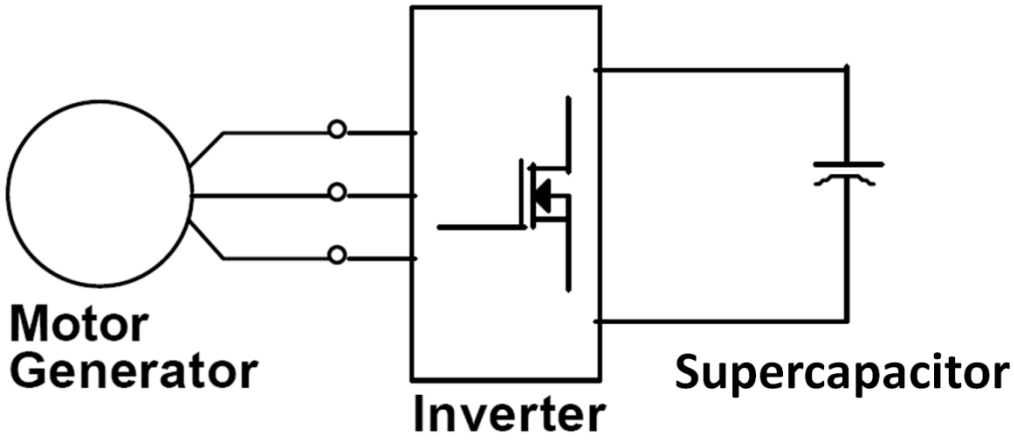

Figure 56: Supercapacitor system with switch mode rectifier in the inverter

4.4 Bidirectional Half Bridge Converter Topology

The half bridge SMPS contains two transistors, a transformer and a rectifier. It has traditionally the advantage of less voltage stress on the transistors, which equates to the maximum DC input of the converter. Therefore, it is often found in offline power supplies. The half bridge converter has the distinctive advantage of minimizing core saturation problems as the DC current through the primary coil is zero due to the coupling capacitors in series with the primary coil. As the primary coil is driven in both directions, the full B-H curve of the transformer is utilized, resulting in more effective utilization of the transformer.

Thus, the half bridge converter is typically used for medium to high power applications from 150W to 1kW. [33] The half bridge converter is considered a buck derived SMPS. The supercapacitor SMPS based on the half bridge converter, would therefore share the same characteristics and is still capable of higher power ratings as compared to the typical buck converter, at the expense of an additional transformer. Figure 57 describes a multiple input bidirectional half bridge converter [37], which is able to incorporate multiple input power sources, such as fuel cell, battery or other electrical sources.

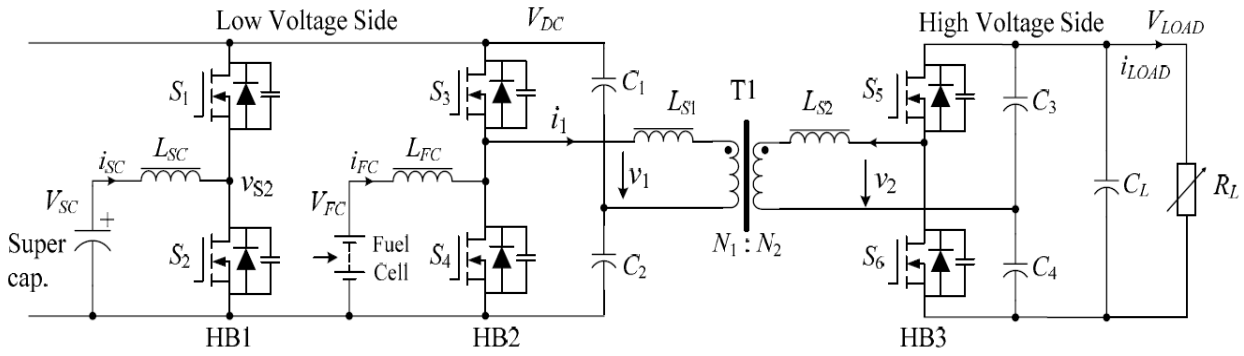

Figure 57: Multiple input half bridge [37]

4.5 Bidirectional Full Bridge Converter Topology

The full bridge SMPS contains two switching legs. Thus, it draws two current pulses from the input voltage source per transistor switching cycle. The voltage stresses of the switches equal to the maximum input voltage, the similar to the half bridge converter, the full bridge converter uses the primary coil from both directions. Thus, the transformer of the full bridge SMPS is effectively utilized. While it shares some similarity to the half bridge converter, it is often used in much higher power applications, typically from 500W to 5kW. Most very high power SMPS would use the full bridge converter topology. Figure 58 shows a schematic of a bi-directional voltage fed full bridge converter [38].

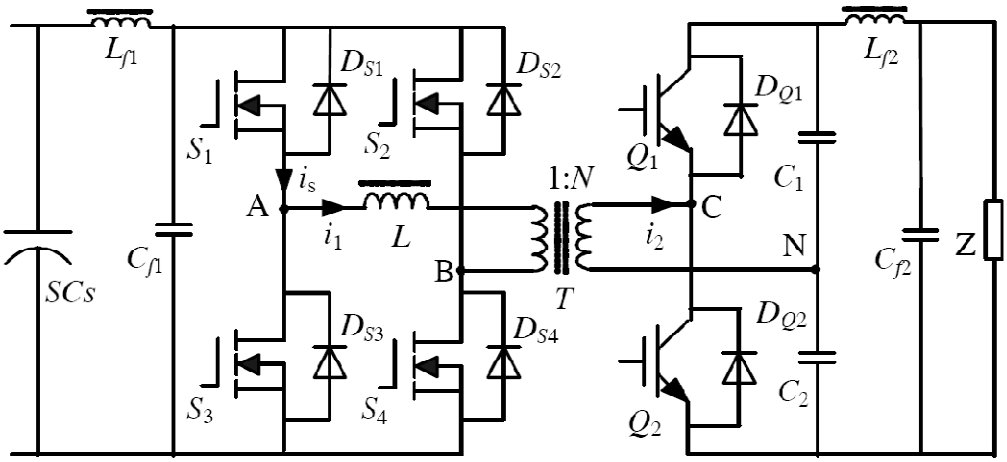

Figure 58: Bidirectional voltage fed full bridge with voltage doubler [38]

Full bridge converter traditionally is more efficient towards the higher power ratings. Thus, for very high power applications, the full bridge converter derived SMPS would be ideal for use in the supercapacitor system.

4.6 Bidirectional Hexa-Mode Buck-Boost Converter Topology

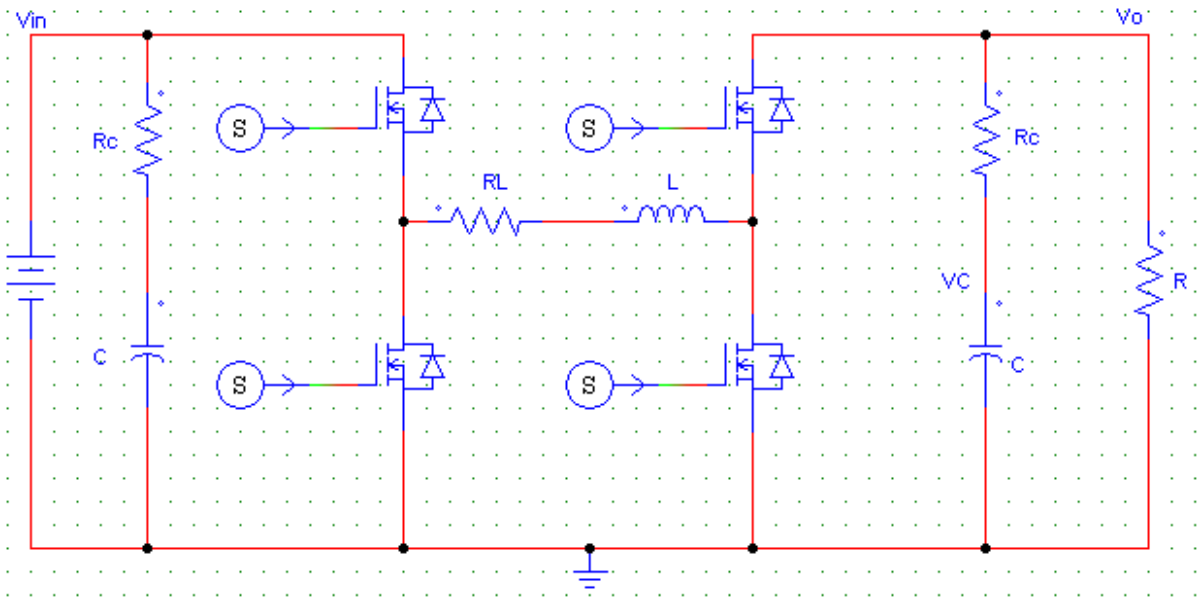

Figure 59: General schematic of the bidirectional hexa-mode buck-boost converter

The hexa-mode buck-boost converter topology has the advantage of being extremely versatile, by virtue that it can operate in buck, buck-boost and boost mode in either direction, therefore the term hexa-mode. It is termed the hexa-mode converter thereafter. It allows a supercapacitor module of any voltage to be incorporated to implement an energy buffer application, regardless of the value of regulated voltage. Such an application cannot be achieved using the bidirectional buck-boost converter topology. While it contains two more switches as compared to the bidirectional buck-boost topology, it may be worthwhile in many applications due to the additional flexibility.

Some applications such as motor control requires the SMPS to output a variable voltage, at times higher or lower than the supercapacitor voltage. While it may be argued that the bidirectional buck-boost topology may be the simplest to implement due to the least number of components required, this topology is undeniably the most versatile.

4.7 Generalization of Supercapacitor Topology

It is noted that most SMPS based topology are not application specific. A fuel cell can also be used in place of the battery, and vice versa. The bidirectional SMPS topology which is popular in the application of automotives can also be used in the micro-grid and other applications with appropriate scaling done. As such, development of the supercapacitor based SMPS is crucial to the general implementation of supercapacitor system as a whole.

Figure 60 and Figure 61 show the typical connection of the supercapacitor, with Figure 60 being the series or cascade method of implementing the supercapacitor [38]. Figure 61 shows the implementation of supercapacitor in parallel to the DC power source [34].

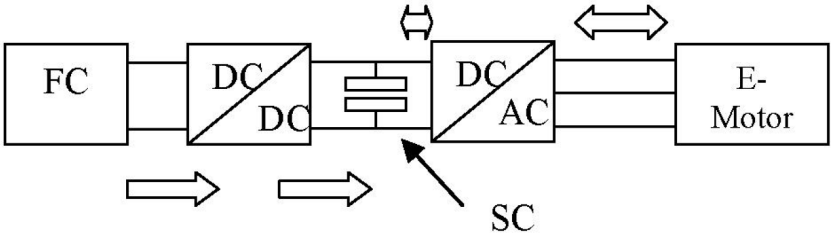

Figure 60: Block diagram of fuel cell coupled with supercapacitor in series/cascade mode

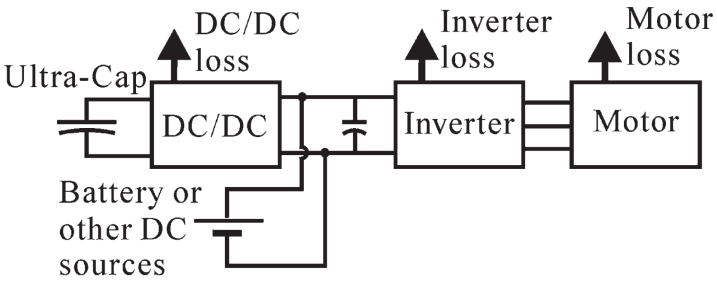

Figure 61: Conventional supercapacitor interface in parallel mode [34]

The series or cascade mode is easy to implement. That is mainly due to that the SMPS often has to be only unidirectional. Control algorithm is also simplified due to that the control system are cascaded, therefore interaction between control algorithms are minimized. The parallel mode is often more difficult to implement as the supercapacitor and other DC sources are connected in parallel. Because the DC sources and supercapacitor are usually of different voltage rating, they typically employ SMPS coupling to achieve common output voltage.

To realize the full potential of the supercapacitor, the coupling SMPS has to be bi-directional in nature. This is to ensure that besides discharging the supercapacitor, the supercapacitor can also be charged. Although the series or cascade mode is easier to implement, the system is significantly less versatile as compared to the parallel mode as it is unable to control when to charge or discharge the supercapacitor. This implies that it is only capable of performing passive peak load shaving. The parallel mode allows the full charge or discharge of

supercapacitor independently, which is the fundamental of active peak load shaving. Therefore, despite the difficulty in implementation, the parallel mode saw widespread use in computer power supplies, UPS and other applications.

4.8 Possible Topology for Highly Fluctuating Load

Most topologies researched to date revolve about the supercapacitor in use together with a battery or fuel cell source. Supercapacitors are usually not the main energy storage device, but the batteries are. Obtaining stable power output from voltage fluctuating source is often an issue, such in the case of regenerative braking or wind turbines. Therefore, supercapacitor can be used to buffer the energy delivery.

Whilst some applications require the supercapacitor voltage to be permanently lower than the regulated voltage, there are some applications where the supercapacitor voltage can fluctuate to be larger or smaller than the regulated voltage. This scenario typically occurs when the regulated voltage is low, such as the UPS for data storage devices. Most SMPS topology discussed earlier do not allow that, with the exception of the hexa-mode converter topology. This justifies the claim that the hexa-mode buck-boost topology is indeed the most versatile bidirectional topology.

4.9 Principle of Hexa-Mode Buck-Boost Converter Topology

The presence of two more switches on the bidirectional hexa-mode converter compared to the bidirectional buck-boost converter gives it the ability to operate in the buck, buck-boost and boost mode in either direction, a total of 6 modes. While SMPS can traditionally operate in

either Continuous Conduction Mode (CCM) or Discontinuous Conduction Mode (DCM), it is assumed that the converter in discussion is always operating in the CCM. That is, the inductor current is always continuous and therefore more than 0. Figure 62 shows the hexa-mode converter operating in boost mode while Figure 63 shows the hex-mode converter operation in the buck-boost mode. While both figures show energy transfer in only one direction, reverse energy transfer is permissible by sending the complimentary switch signal, due to the symmetry of schematic design.

Rightfully, the system is already very versatile by simply implementing the buck-boost mode, as it can cater to higher or lower input voltage ratings compared to the output. In such a scenario, operation in the buck or boost mode are not required. However, it was discovered that the buck-boost mode suffers from low efficiency at high gain when output current draw is high. This result in very limited DC voltage gain when the input voltage is low compared to the output voltage.

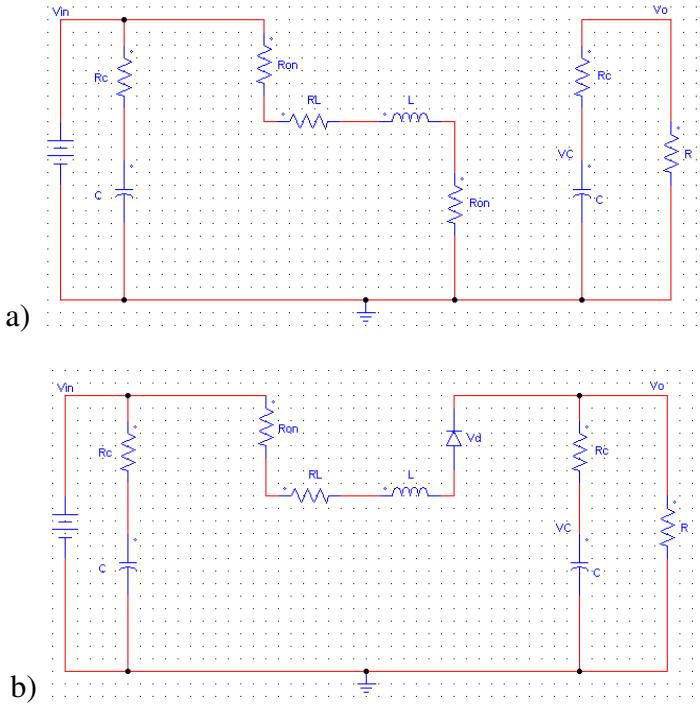

Figure 62: Schematic of the bidirectional hexa-mode controller in boost mode

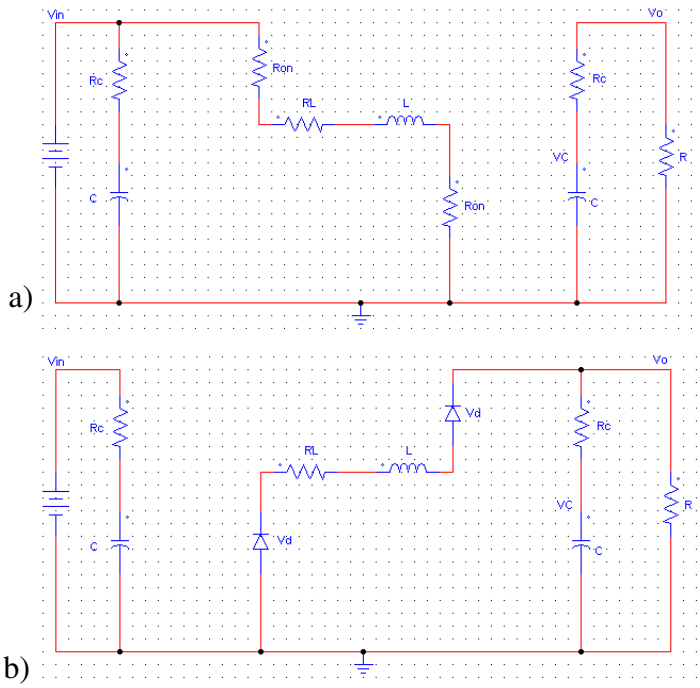

Figure 63: Schematic of the bidirectional hexa-mode controller in buck-boost mode

The ideal DC voltage transfer function, also known as the DC voltage conversion ratio or DC voltage gain of the buck-boost converter is:

$$\frac{V_O}{V_{in}} = \frac{D}{1-D}, \text{ where } V_O \geq 0 \text{ and } V_{in} \geq 0 \quad . \tag{20}$$

However, by taking parasitic such as the inductor ESR R_L, diode forward voltage drop V_d as well as the on resistance of the MOSFETs R_{on}, the DC transfer function becomes:

$$V_O = \frac{(-i_o R_L - 2Di_O R_o n - 2V_d + 4DV_d - 2D^2 V_d + DV_i n - D^2 V_i n)}{(-1+D)^2}, \text{ where } V_O \geq 0 \text{ and } V_{in} \geq 0 \,. \tag{21}$$

It can be quickly noted that the parasitic components can severely affect the output voltage gain. While the diode forward voltage drop is consistent, the MOSFET on resistance and inductor ESR can contribute to a lot of loss that affects the output voltage gain. This condition occurs when the duty ratio is high, which also implies higher inductor current for

the same output current. The later is evident as for a buck-boost converter, the inductor current is denoted by

$$i_L = \frac{I_O}{(1-D)} = \frac{I_{in}}{D} \quad , \tag{22}$$

where, i_L is the inductor current, I_O the output current and D the duty ratio.

Therefore, the DC current transfer function is denoted as:

$$\frac{I_O}{I_{in}} = \frac{1-D}{D} \quad . \tag{23}$$

When the parasitic $V_d = 0.4V, R_{on} = 0.058\Omega \; and \; R_L = 0.1\Omega$ are added, the voltage gain curve changes as observed in Figure 64.

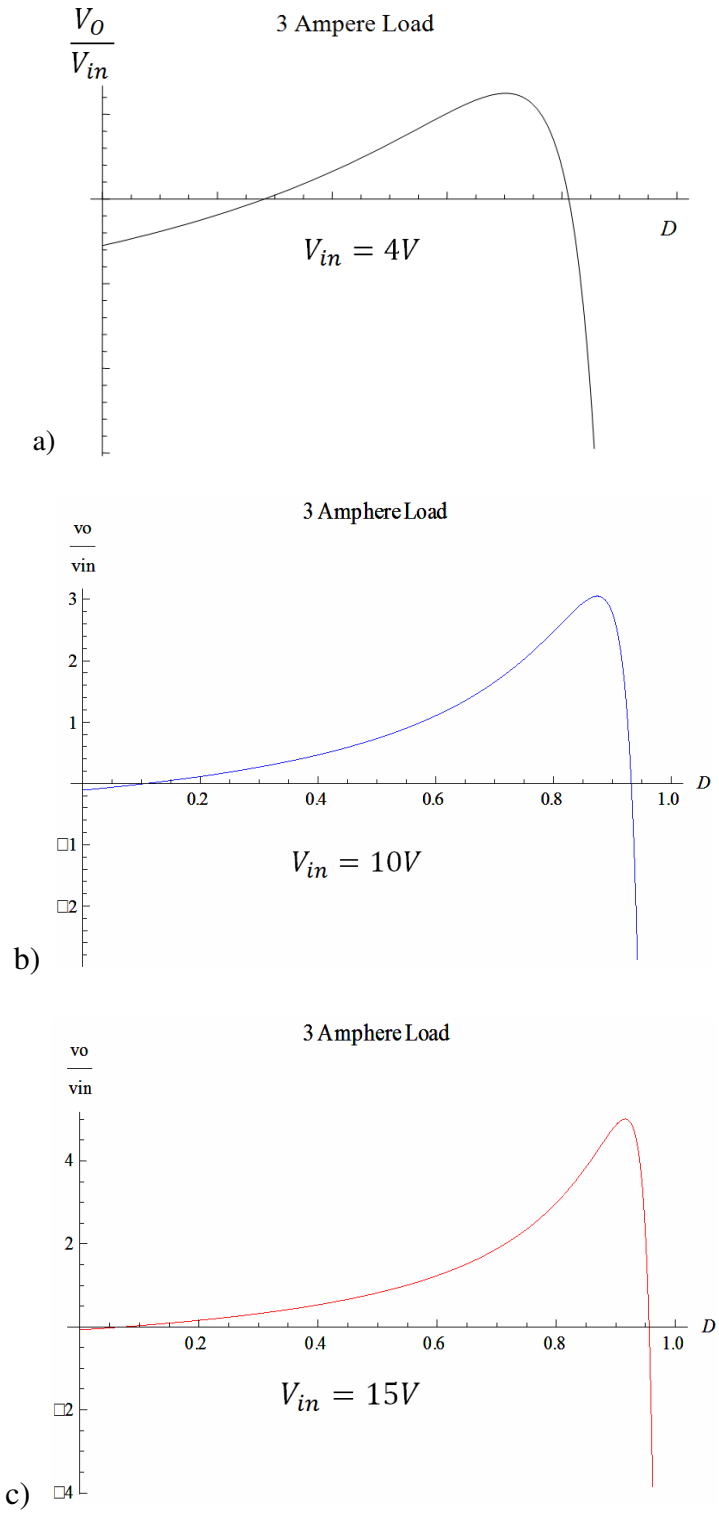

Figure 64: $\frac{V_O}{V_{in}}$ ratio of buck-boost converter under constant current load of 3A when $a) V_{in} = 4V$, $b) V_{in} = 10V$ and $c) V_{in} = 15V$

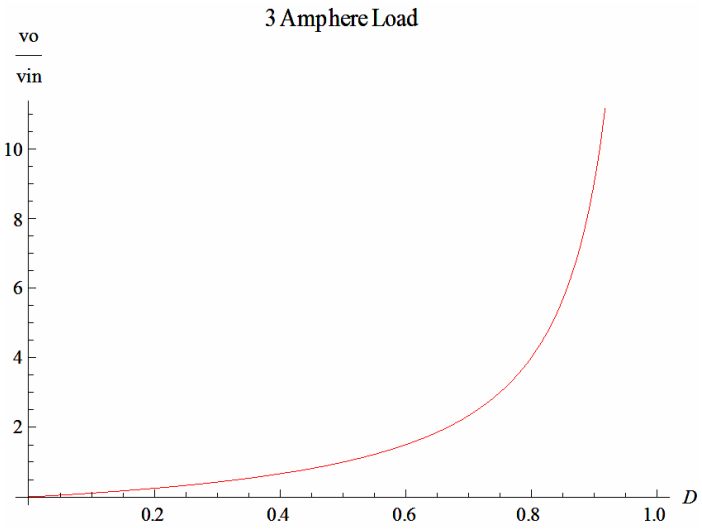

Figure 65: $\frac{V_O}{V_{in}}$ ratio of buck-boost converter with no parasitic regardless of load current and input voltage

Figure 65 shows the mathematical plot of (21) without taking into account parasitic while Figure 64 took parasitic into account. All the plots are produced using the software Mathematica 7.0 from Wolfram. In Figure 64, the curve turns into negative DC gain when the duty is very small or very high. This occurs when the converter is unable to produce the output current demand. This is especially pronounced when V_{in} is small, as observed in Figure 64. It has to be noted that it is not possible to achieve negative output voltage due to the blocking diodes. As such, the curve is only applicable when the DC gain is positive.

It can be noticed that the higher the current load the more pronounced the parasitic affects the voltage gain. Figure 66 shows the efficiency curve of the converter based on (24).

$$\eta = \frac{V_O i_O}{V_{in} i_{in}} = \frac{-i_o R_L - 2Di_O R_{on} - 2V_d + 4DV_d - 2D^2 V_d + DV_{in} - D^2 V_{in}}{D(-1+D)} \quad , \tag{24}$$

where, η is the efficiency of the converter.

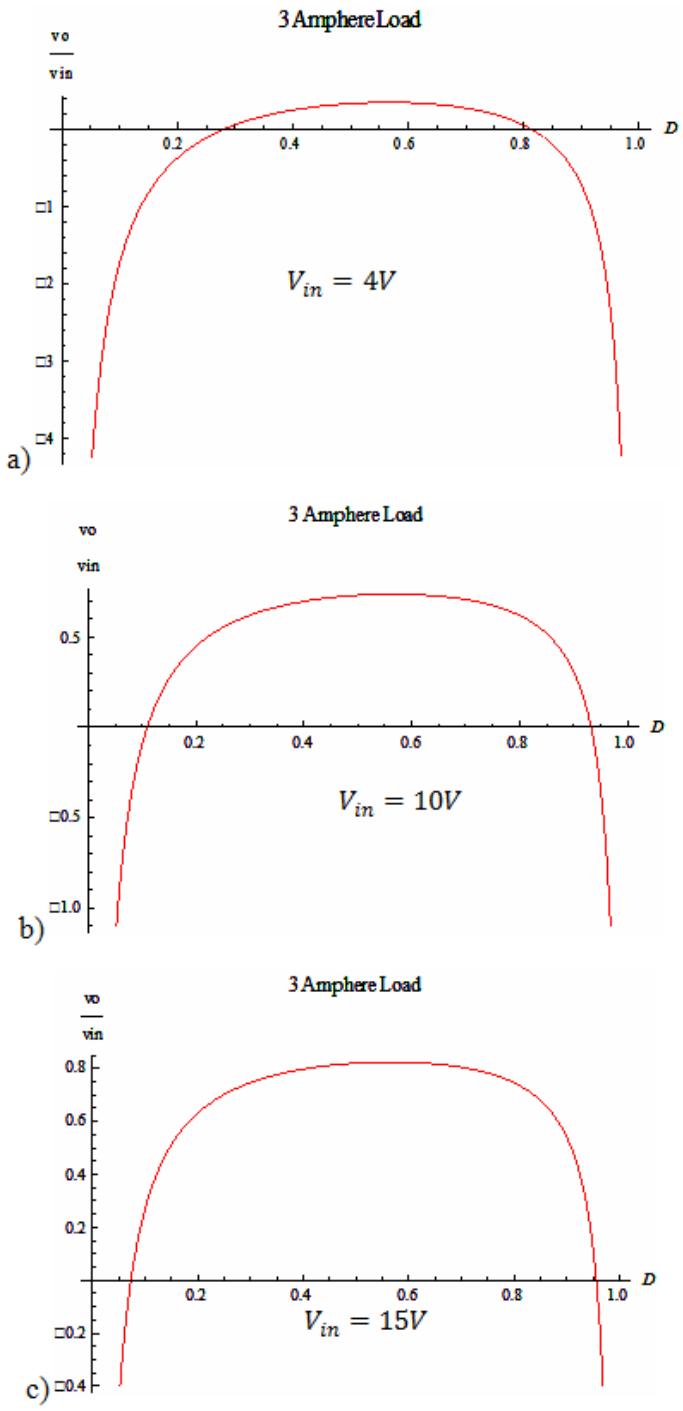

Figure 66: Efficiency curve of bidirectional converter when under constant current load $a)V_{in} = 4V$, $b)V_{in} = 10V$ and $c)V_{in} = 15V$

Again, the efficiency cannot be negative in this case. It was caused by the inability of the converter to provide the output current demand at the respective duty ratio. Only when the efficiency is positive are the values are meaningful. Minimization of the parasitic values can

reduce the issue, but in general, components are fixed due to constrains such as availability, footprint, pricing and other factors. Therefore, the parasitic values are often not selectable.

As such, some topology can be used to boost the output voltage of the converter operating in buck-boost mode. One such way is to incorporate the boost mode. However, the boost and buck-boost modes are vastly different models. Whilst trying to keep control as simple as possible, it is not advisable to operate with two distinct models. As such, it is possible to incorporate a model that contains both the buck-boost and boost mode as an intermediate between the boost and buck-boost mode. This model is termed the hybrid mode.

4.10 Hybrid Model

While most SMPS operates in the bi-state, some tri-state SMPS are available. In order to bridge both the buck-boost and boost modes, it is possible to incorporate a boost mode state into the buck-boost state to produce a tri-state that contains both buck-boost and boost elements. Achieving this hybrid state can further boost the DC voltage gain with little change in state equations.

It can be observed that for this system operating in CCM,

$$\alpha + \mathrm{D} \leq 1 \quad . \tag{25}$$

When $\alpha + D = 1$, the system migrates into a pure boost mode.

The output current, i_O, for such a system can be estimated to be:

$$i_O = (1 - D) i_L \quad . \tag{26}$$

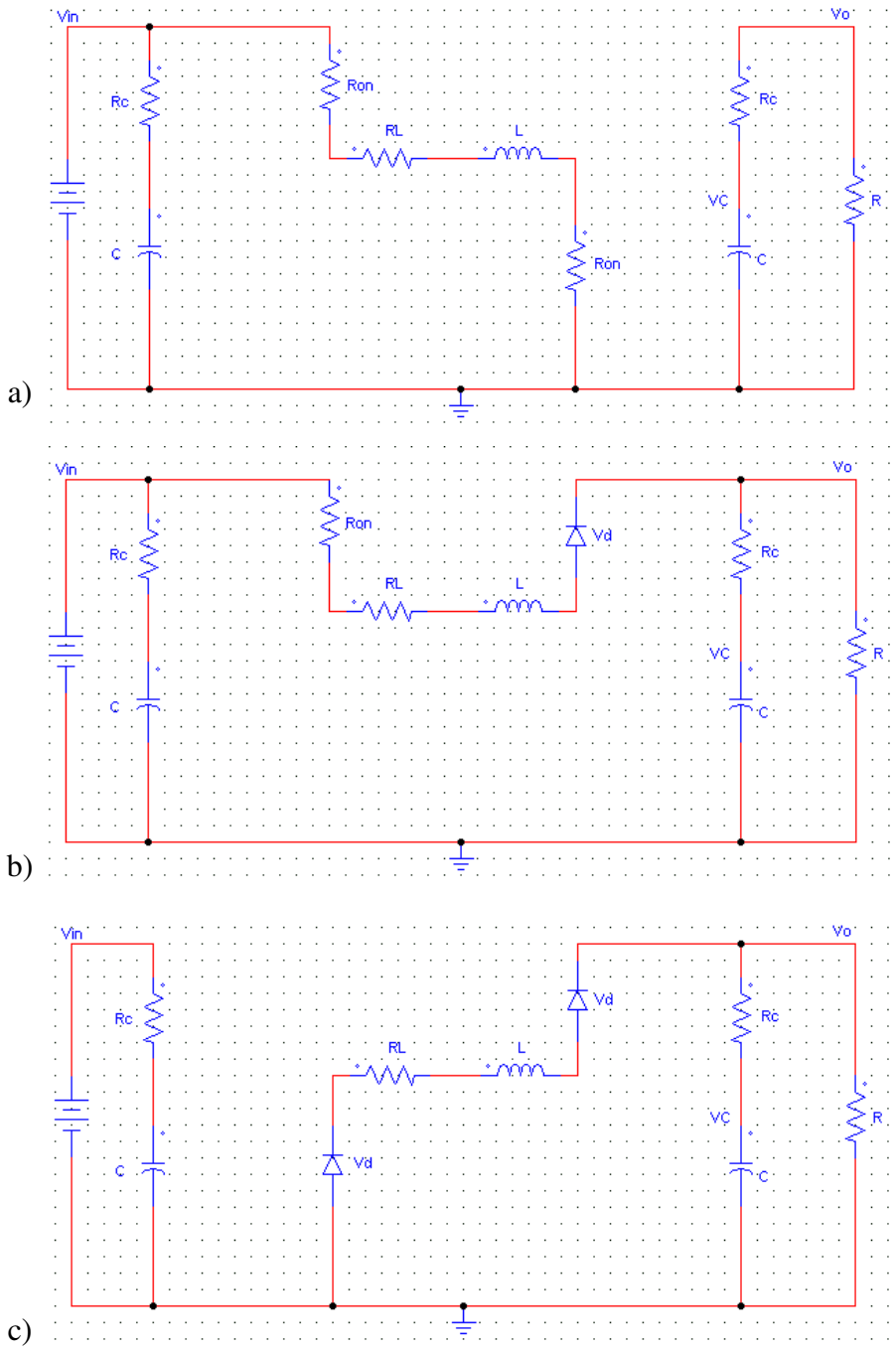

Figure 67: Hybrid State consisting of buck-boost and boost states, a) The *D* stage, b) The α stage and c) the 1-D-α stage

While there are several ways to model the SMPS, the state space averaging technique is employed here, as the state equations are readily implemented in simulation software like

MATLAB. The small signal model as well as DC transfer function was derived in Appendix A.

The DC Transfer function can be denoted as:

$$V_O = \frac{i_L R_L + \alpha i_L R_{on} + 2D i_L R_{on} + 2V_d - \alpha V_d - 2DV_d - \alpha V_{in} - DV_{in}}{(-1+D)} \quad . \tag{27}$$

Removing the parasitic terms, the ideal DC transfer function is denoted as:

$$\frac{V_O}{V_{in}} = \frac{\alpha + D}{(1-D)} \quad . \tag{28}$$

It can be observed that when $\alpha = 1 - D$, the transfer function becomes that of the boost mode. Analytically, the hybrid state would modify the inductor waveform as observed in Figure 68 and Figure 69.

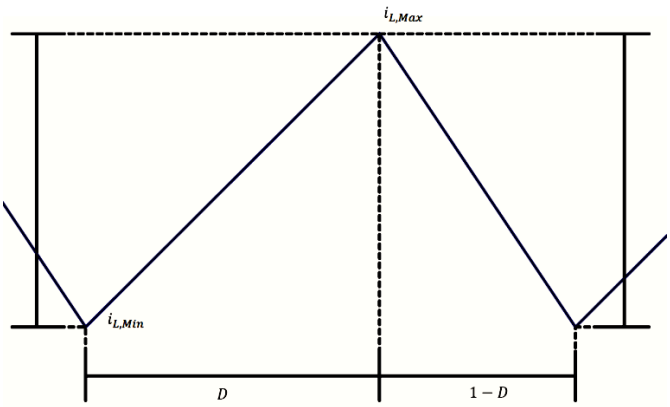

Figure 68: Typical inductor current of the hexa-mode converter in CCM

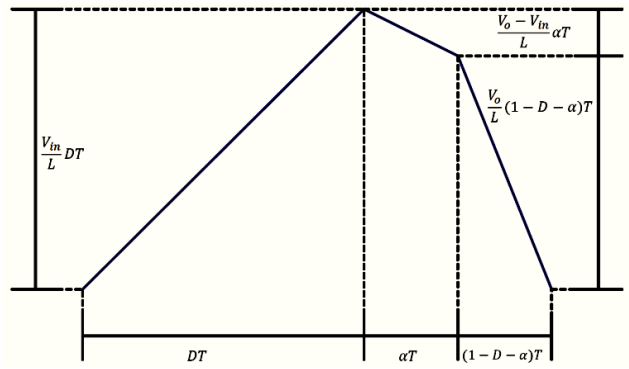

Figure 69: Inductor current waveform of hexa-mode converter operating in hybrid state

4.11 Calculation and Selection of Components for Hexa-Mode SMPS

The hexa-mode converter is made to operate to the following requirements:

$0.5A < I_O < 5A, V_O = 12V, 4V < V_{In} < 15V, f_s = 50Khz,$

The CCM/DCM boundary occurs at $I_O = 0.5A, V_{In} = 15V, V_O = 12V$ when the converter is operating in the buck-boost mode. Therefore, the boundary inductor current $\mathrm{I_{L,min}}$ is

$$\mathrm{I_{L,min}} = \frac{\mathrm{I_O}}{(1-\mathrm{D_{min}})} \quad . \tag{27}$$

During the T_{on} state,

$$\mathrm{L}\frac{\mathrm{di_L}}{\mathrm{dt}} = \mathrm{V_{in}} - 2\mathrm{i_L R_{on}} - \mathrm{i_L R_L} \quad . \tag{28}$$

During the T_{off} state,

$$\mathrm{L}\frac{\mathrm{di_L}}{\mathrm{dt}} = \mathrm{V_O} + 2\mathrm{V_D} + \mathrm{i_L R_L} \quad . \tag{29}$$

Using the conservation of current during continuous conduction mode, the following result can be obtained,

$$\frac{V_O + 2V_D + i_L R_L}{V_{in} - 2i_L R_{on} - i_L R_L} = \frac{D}{1-D} \quad . \tag{30}$$

Substituting (41) into (44), we have

$$\frac{V_O + 2V_D + i_L R_L}{V_{in} - \frac{i_o(2R_{on} + R_L)}{1-D}} = \frac{D}{1-D} \quad . \tag{31}$$

At CCM/DCM boundary, the inductor current, i_{LB}, barely reached 0 in the dynamic state. Therefore, $\Delta i_{LB} = 2 \times i_{L,min}$, corresponding to D= 0.465843.

At CCM/DCM boundary, $\Delta i_L = 2i_L$. Considering the T_{on} interval, we have

$$L\frac{di_L}{dt} = Vin - 2i_L R_{on} - i_L R_L \quad , \tag{32}$$

and

$$L_{min} = \frac{(Vin \bullet D - 2i_L R_{on} \bullet D - i_L R_L \bullet D)}{2i_L \bullet f_s} = 74.2\mu H \quad . \tag{33}$$

The MOSFET chosen was International Rectifier's IRFI4212H, rated at 100V and 11A. The 50WQ04FN from Vishay houses two Schottky diodes each with forward voltage drop of 0.4V. Each diode is rated to 5.5A continuous with 40V rated reverse voltage. This diode package allows the chip to handle 11A of continuous current.

The fundamental hardware of the converter is as follows:

1) 470uH Inductor, with 100mΩ ESR
2) Analog Devices ADMC401 DSP
3) 2200uF capacitor with 4mΩ ESR
4) 50WF04FN Schottky diode with forward voltage of 0.4V
5) IRFI4212H – MOSFET with $R_{on} = 0.058$

4.12 Simulation of Hexa-Mode SMPS

To investigate the operation waveforms of the hexa-mode SMPS, the average model (derived in Appendix A) was used to implement the simulation in SIMULINK. The average model is:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{On}(2D+\alpha)+R_L+a\bullet R_C\bullet(1-D)}{L} & -\frac{a}{L}(1-D) \\ \frac{a}{C}(1-D) & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{D+\alpha}{L} \\ 0 \end{bmatrix} V_{In} - \begin{bmatrix} \frac{2-2D-\alpha}{L} \\ 0 \end{bmatrix} V_D \quad (34)$$

Figure 71 shows the implementation of the equation in SIMULINK while

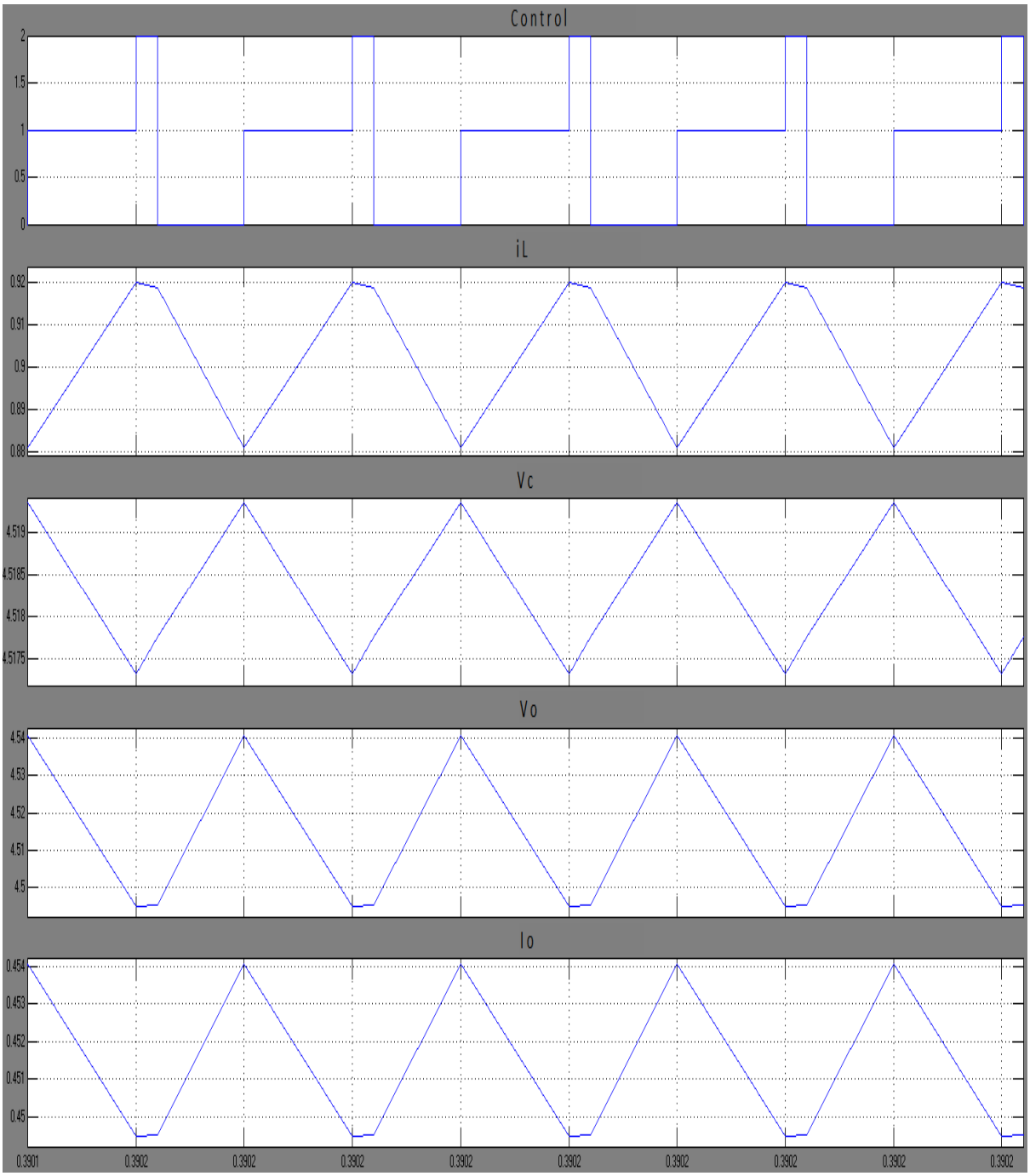

Figure 70 shows the simulation results. The system was made to operate in the D state when the Control signal is of magnitude 1, α state when the Control signal is of magnitude 2 and the (1-D-α) state when the Control signal is of magnitude 0. The simulated inductor waveform is indeed as predicted in Figure 69.

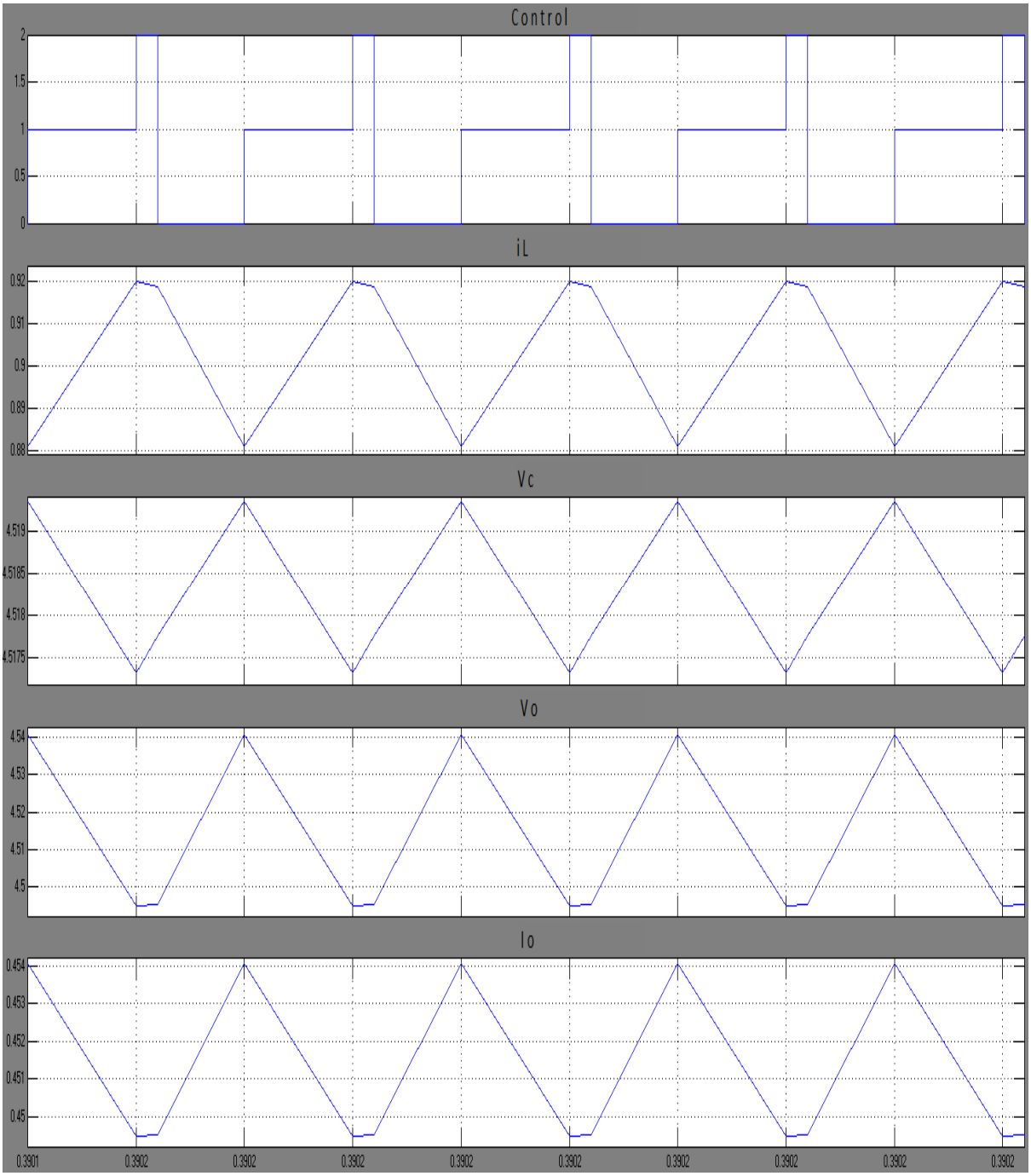

Figure 70: Simulation of hexa-mode converter in hybrid state

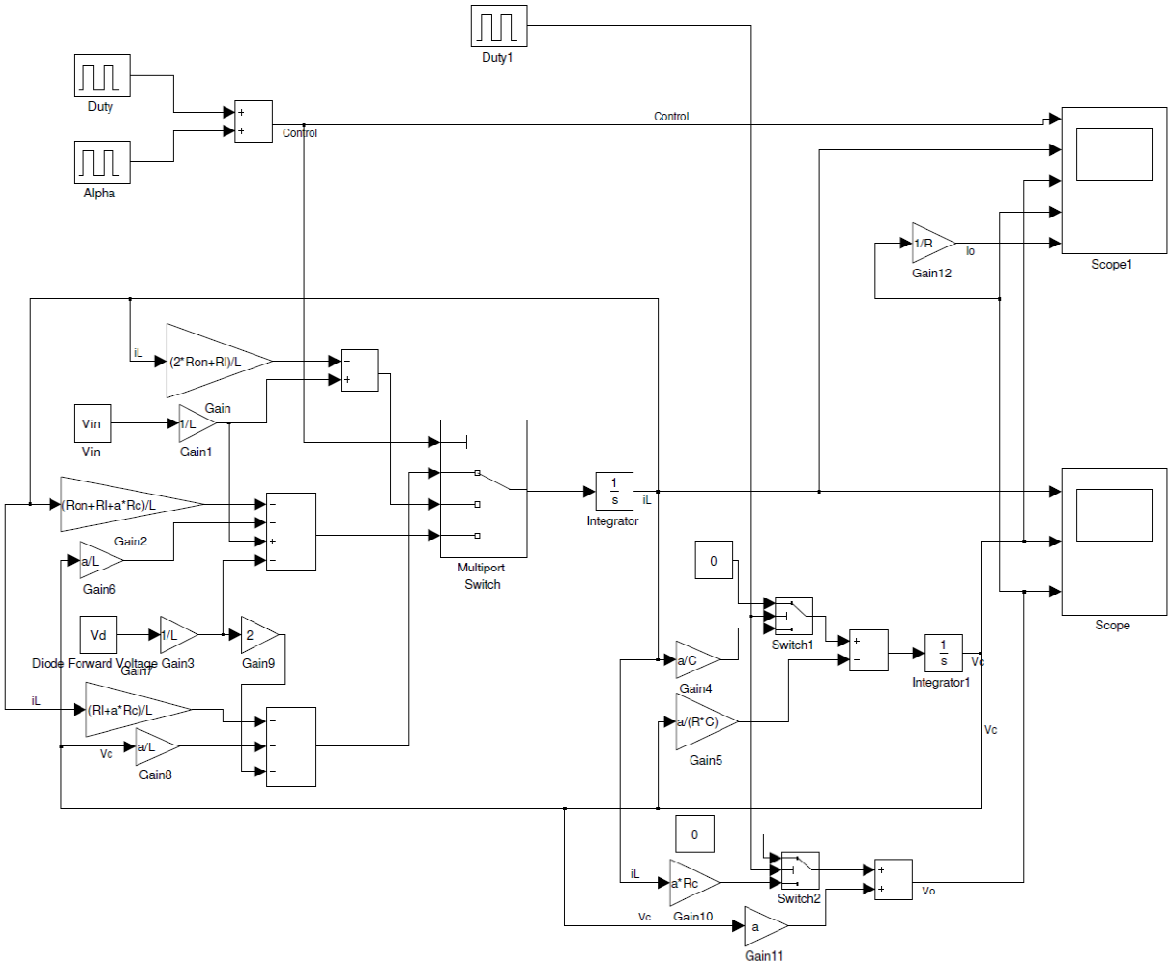

Figure 71: Hexa-mode converter - Simulation (SIMULINK) model

4.13 Utilizing the Hybrid State

Consider a 5.5V supercapacitor having to supply 5V of voltage to a HDD through the hexa-mode converter, and having to sustain the 5V regulation till 2V in terminal voltage. Such a converter would be made to operate in the buck-boost mode, followed by the hybrid state and eventually if need be, the boost state.

To simplify the controller design, the system is made to operate in the buck-boost mode for up to D=0.5. After which, D is made to operate constantly at 0.5, while α would start

operating from α=0 to a maximum of α=0.5. Upon reaching α=0.5, the system is then operating in the pure boost mode. Once this happens, T1 is permanently closed whilst T3 is controlled by the duty cycle D.

As the bidirectional circuitry is symmetrical, evaluating the converter in a single direction is equivalent to evaluating the converter in the opposite direction. Therefore, the same model can be used for charging and discharging the supercapacitor.

4.14 Chapter Conclusion

A number of bidirectional SMPS voltage regulators are proposed for use with supercapacitor due to the fact that the parallel topology is preferred over the series or cascade variants for the flexibility of implementing the active peak load shaving topology. While some very popular topology such as the bidirectional buck-boost converter has the advantage of operation with less components, it is unable to output voltages lower that of the supercapacitor voltage. The hexa-mode converter, however, has no such limitations.

A thorough analysis of the hexa-mode converter is presented, where the converter characteristics were derived and simulation was done to reaffirm the understanding. Due to the need to operate in buck-boost and boost mode, a tri-state mode bridging both modes was derived and termed the hybrid mode. The hybrid mode is a combination of states from the buck-boost and boost mode, which becomes the buck-boost mode when α=0, while it turns into the boost mode when α=1-D. The hybrid state offers higher DC voltage gain compared to the buck-boost mode and offers seamless transition from the buck-boost mode to the boost mode.

Chapter 5

Practical Implementation of Bidirectional SMPS with Supercapacitor

5.1 Introduction

This chapter describes the algorithm used to implement the hexa-state converter, and the ADMC 401 DSP onboard is used as the master board. The schematic of the daughter board containing the hexa-mode converter was shown in Appendix C. This non-isolated converter is chosen due to its ability to operate in all 4 quadrants. This converter is especially important if the supercapacitor operation voltage is allowed to be higher or lower that of the regulated voltage. The reverse is true as well: This converter allows load voltages of higher or lower voltage relative to the supercapacitor to charge it. As charging was involved, the hexa-mode converter was made to be able to operate in the constant current mode. This enables the supercapacitor system to operate in the acceptable current condition. The experiments were designed to demonstrate this ability. The converter with supercapacitor is then applied to the HDD to achieve UPS functionality to some potential of the possible applications.

5.2 Experimental Setup

Supercapacitor - The BPAK0058 E015 B01 Supercapacitor module from Maxwell Technologies was chosen due to the active balancer that comes onboard the module. It is

rated at 15V and 58F. The capacitance is sufficiently high to perform some significant energy operations.

Digital Processor - The electronic schematics in Appendix C were designed to accommodate the DSP board which acts as a master board. As such, it is termed a daughter board. Components such as opto-couplers (both analog and digital) have been used to achieve isolation between the control circuitry and power electronics, so as to protect the control circuitry should a electrical runaway take place. To improve noise immunity, critical signals undergo differential pair transmission at/near the source, which is then subtracted at the DSP. By subtraction of the acquired data pair, common mode noise is removed.

DC Source - The experimental DC source is a Kenwood PD35-10 laboratory DC power supply. This power supply has a constant current limiter onboard, which was handy in preventing experimental/thermal runaways. Also, controlling the knob can simulate a voltage source with varying current output, which is useful to evaluate the peak load shaving performance of the supercapacitor system.

Electrical Load - To maintain ease of experiment, the IT8514C programmable electronic load from ITECH acts as the electrical load. The IT8514C can operate in constant power mode, constant current mode, constant voltage mode and constant resistance mode, which is a lot faster to tune, easier to operate and safer as compared to heating up resistor loads. IT8514C is rated at 1200W 120V/240A, which exceeds the specifications needed for the experiments.

With the hardware equipments and components in place, the system implementation is largely dependent on the DSP program, which dictates how the system should behave and

respond. The DSP program is implemented in assembly language, which allows tight control over the clock cycles used to implement each function and as well as function priority.

5.3 DSP Control Algorithm

The ADMC401 onboard the master board is a DSP from Analog Devices that operates at a maximum of 26 MIPS. It comes with internal Analog Digital Converter (ADC) which makes it the ideal device for acquiring voltage and current signals from the SMPS. By using such a DSP, comparator based control such as peak current mode control would not be applicable due to insufficient ADC sampling rate. Also due to insufficient ADC sampling rate, cycle by cycle regulation is not possible. However, such a system is sufficient to implement average voltage and current control topology, which suffice for energy transfer to and fro the Supercapacitor. The DSP Printed Circuit Board (PCB) is modified internally to operate at 20 MIPS and is configured to operate as a master board. The bidirectional SMPS is located at the daughter board. The following lists the main functions of the DSP algorithm.

5.4 Initialization

This is the fundamental function of the DSP where declarations and routines are set. The PWM is set to operate in crossover mode at a frequency of 50 KHz with both the crossover and double update mode. This is due to that for this application, the crossover mode is the most optimum way to implement the PWM. Operating in the double update mode allows the PWM interrupt to occur at 100 KHz rate, doubling the PWM resolution.

The ADC is set to operate in the simultaneous sampling mode, where the 8 individual ADCs are sampled in pairs. This is utmost crucial as the feedback signal to the DSP are in the form of differential pairs. The DSP requires 2.45μSeconds to sample four pairs of ADC, after which a dedicated ADC interrupt is generated.

5.5 Digital PI Control

To achieve voltage or current regulation in the hexa-mode converter, the DSP has to incorporate a control scheme. While traditional controllers are made possible via the combination of passive components such as capacitors, resistors and operational-amplifiers, the performance suffers drift due to component degradation with aging effect.

Digital control is made possible via the implementation of digital processor in place of the passive components. Operands such as addition, multiplication etc are performed in the processor as opposed to passive components. While performance do not suffer from drift due to component aging, they can also be tuned to handle variations in almost any methods wanted. Digital control is chosen to be implemented in the system due to flexibility and ease of tuning.

While many controllers are available today, PI controllers are widely known and implemented in various systems due to their flexibility and easiness to tune. PI controllers are typically analyzed and tuned in the continuous time domain, which has the corresponding transfer function:

$$U(s) = (K_p + \frac{K_I}{s}) \bullet I(s) \quad , \tag{34}$$

where I denote the input error and U denote the controller output. S is the laplace variable while K_P and K_I are the proportional and integral parts of the PI controller respectively. The equation can also be written as

$$U(s) = K_p \bullet \omega_{PI} \bullet \left(\frac{\frac{s}{\omega_{PI}} + 1}{s}\right) \bullet I(s), \tag{35}$$

where $\omega_{PI} = \frac{K_I}{K_P}$, typically expressed in rad/s. This transfer function contains a pole in the origin and a zero located at ω_{PI}. It is noted that K_P is responsible for the high frequencies gain. The bode plot of such a converter is as shown in Figure 72.

Digital implementation of PI controller requires the processor to approximate the integral action by a discrete summation. The Zero Order Hold (ZOH) and First Order Hold (FOH) methods are amongst the most popular methods to implement the integral operation.

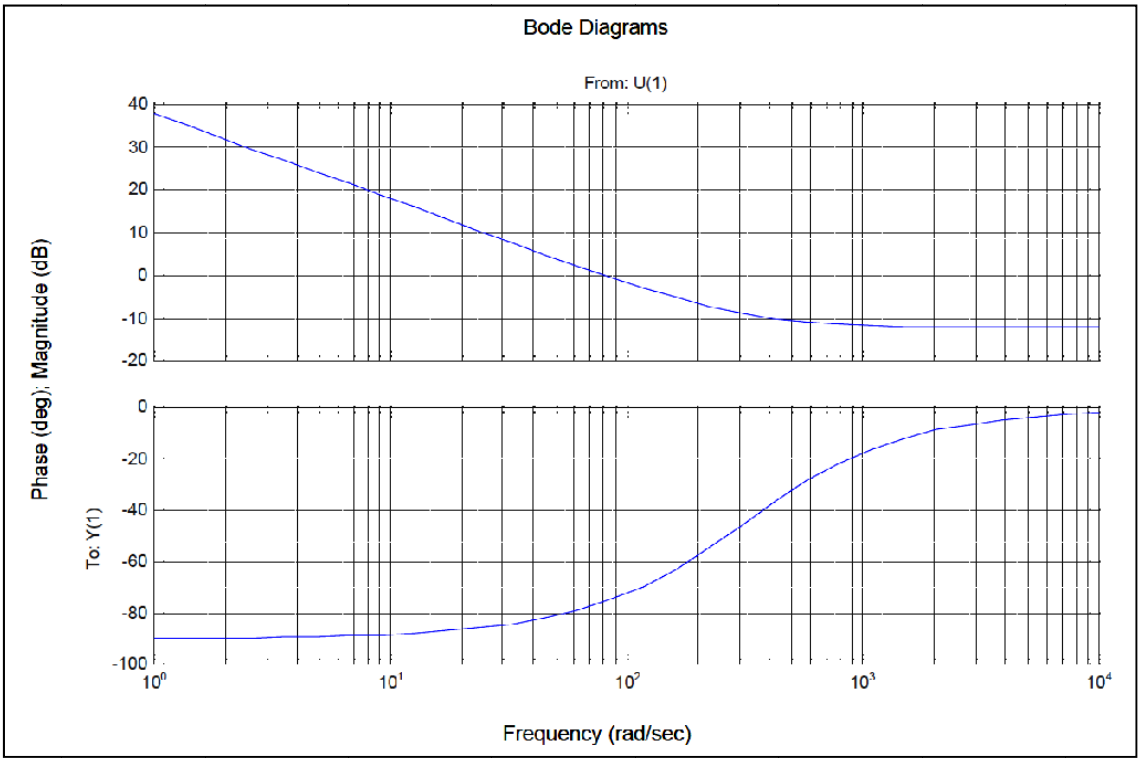

Figure 72: Bode plot of PI controller

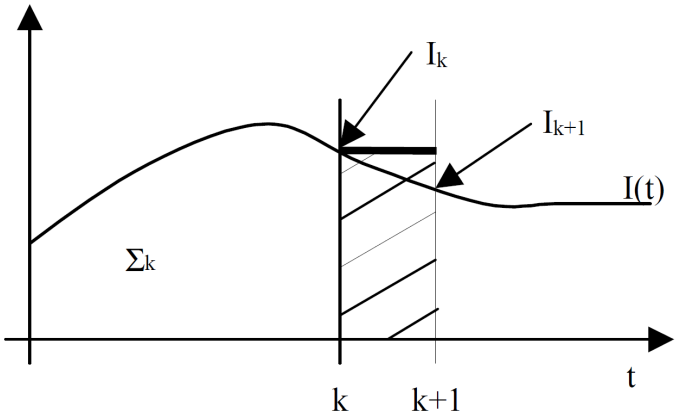

Figure 73: ZOH approximation

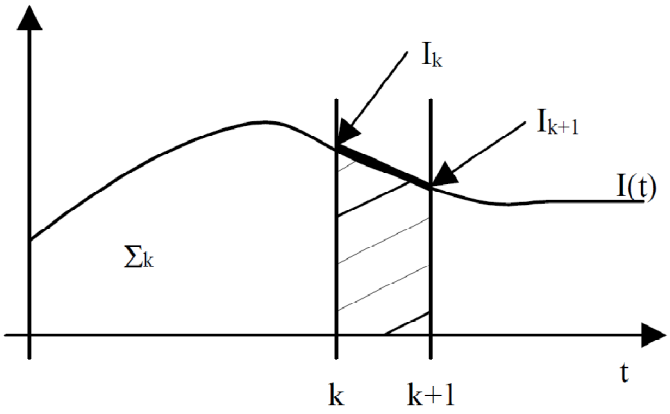

Figure 74: FOH approximation

The FOH is generally a better implementation as compared to the ZOH approximation as the ZOH uses trapezoidal areas to perform integration whereas the ZOH uses rectangular areas. The differences are clearly shown in Figure 73 and Figure 74.

For FOH topology, the integration is done by performing iterations of the following:

$$\sum_{k+1} = \sum_{k} + \frac{I_K + I_{K+1}}{2} \bullet T_{Sample} \quad , \tag{36}$$

where T_{Sample} denotes sample time, $\sum_k$ the sum at instant k, I_K the signal at instant k. The equation can be expressed in the z-domain by:

$$z\sum(z) = \sum(z) + I(z)\frac{1+z}{2}T_{Sample} \quad . \tag{37}$$

Simplifying the above expression, it results in

$$\sum(z) = \frac{T_{Sample}}{2}\frac{z+1}{z-1}I(z) \quad . \tag{38}$$

Transferring the equation,

$$U(z) = K_p\left(1+\omega_{PI}\frac{T_{Sample}}{2}\frac{z+1}{z-1}\right)I(z) = \frac{K_P\left(\frac{\omega_{PI}T_{Sample}}{2}+1\right)z + K_P\left(\frac{\omega_{PI}T_{Sample}}{2}-1\right)}{z-1}I(z). \tag{39}$$

This gives us the difference equation as shown below:

$$U_{k+1} = K_P\left(\frac{\omega_{PI}T_{Sample}}{2}+1\right)I_{k+1} + K_P\left(\frac{\omega_{PI}T_{Sample}}{2}-1\right)I_k + U_k \quad . \tag{40}$$

Based on the mathematical expression in (40), the FOH based PI controller can be implemented on virtually any digital processor.

Constant Voltage Mode Control:

The voltage mode control operates according to the voltage conditions based on the digital PI controller. This mode is responsible for voltage regulation.

Constant Current Mode Control:

The current mode control operates based on the output current directly. The output current is derived from inductor current by using the following relation:

$$I_O = (1-D)I_L .$$

(41)

The constant current mode is responsible for current regulation, mostly used when a current limit is required. In this application, it is used to implement constant current charging of the supercapacitor. This is very crucial in charging because the supercapacitor is able to handle large amounts of current due to its low ESR. Charging in the voltage mode can result in huge amounts of current flowing in the hexa-mode converter which it wasn't designed for. This is very evident due to the very low ESR of supercapacitor.

All supercapacitor charging algorithms in this implementation start with constant current control, and upon reaching the predefined voltage, it switches to the constant voltage mode. This way, there is minimal current surge and current conditions can be controlled to acceptable levels.

PWM Interrupt Routine:

During the PWM interrupt routine, the PWM registers are updated and the corresponding duty ratio is modified accordingly. PWM frequency and other factors are unaffected.

ADC Interrupt Routine:

The ADC interrupt routine is called when the simultaneous sampling of the 4 pairs of ADC has been completed. The binary ADC values are recovered from the differential pair signals, readjusted with the calibrated values and stored in the cyclic memory. After 20 interrupt routine, a user defined ADC flag is raised.

Wait State:

The wait state simply waits for the occurrence of two events, namely the ADC flag and PI control flag. Upon detection of the ADC flag, the ADC average function is called to perform an average of 20 V_{in}, V_o and I_L values each. This updates the V_{in}, V_o and I_L values for use in the digital PI control, and afterwhich the ADC flag is reset.

The PI control flag is set when the timer indicates that it has reached 250 μS or more since the last reset. After the digital PI control function is called, the timer is reset.

ADC Average

This function simply averages the values of V_{in}, i_L and V_O stored in the cyclic memory. Each parameter is the average of 20 ADC capture. This function is only available after the ADC flag is raised, that is, after 20 interrupt routine.

SMPS Mode Selection:

This function determines the operational mode of the SMPS as well as the relevant duty ratio, based on information of $V_{in,}$ i_L and V_O acquired by the ADC. By default, it operates in the buck-boost mode. If the duty ratio exceeds 0.5 in the buck-boost mode, the program calculates if the hybrid state is applicable. If the hybrid state is not applicable, then the boost state is called. All of these update the duty buffer register, from whom the PWM interrupt routine updates from.

It has to be noted that the interrupt routine runs parallel to the normal routine and has higher priority to the normal routine. The DSP algorithm flow chart is as follows:

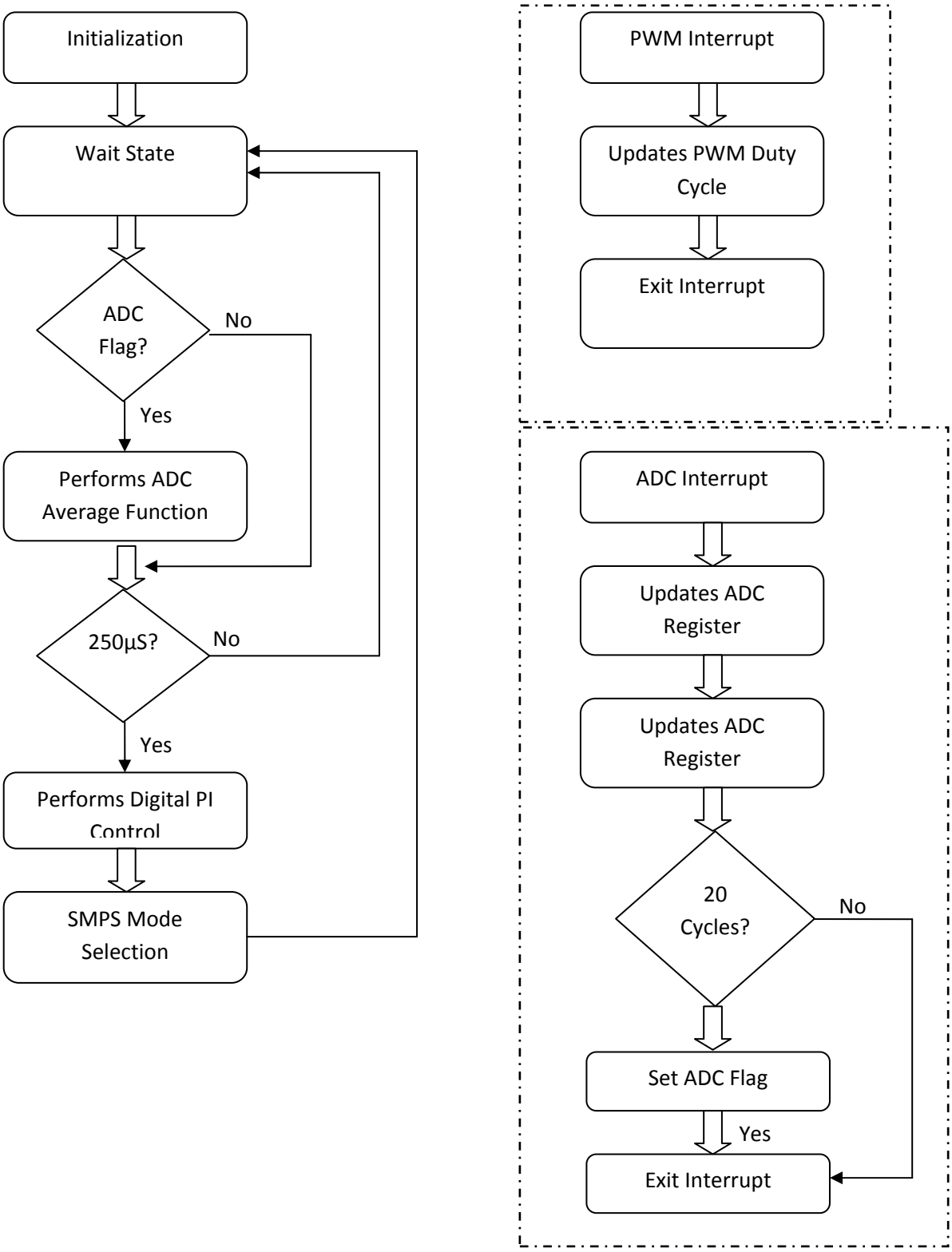

Figure 75: DSP algorithm flow chart

Figure 76: The BPAK0058 supercapacitor module

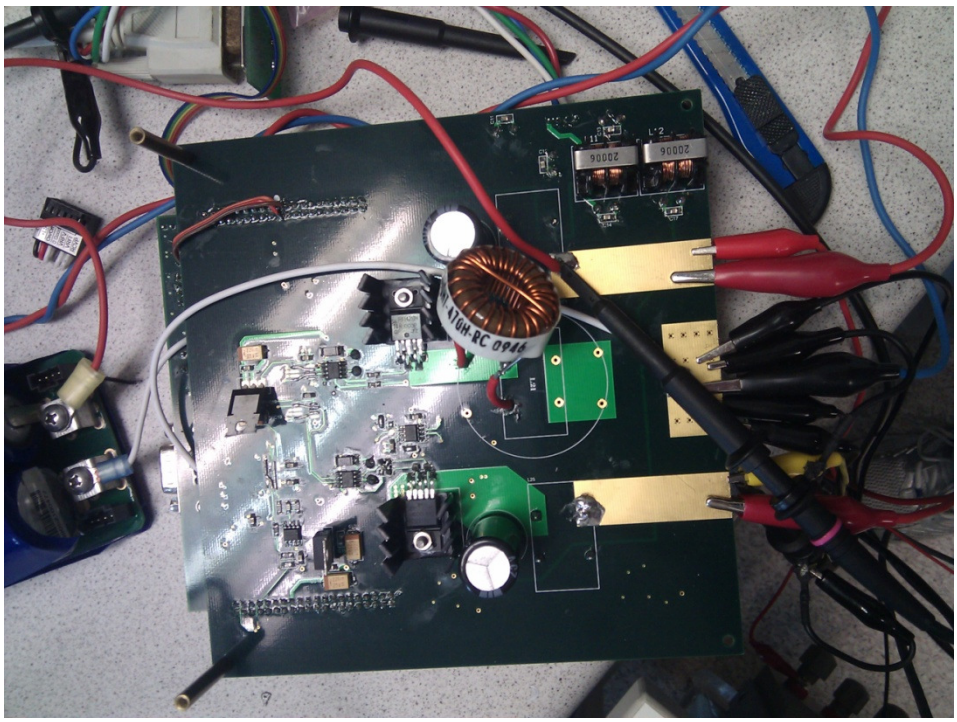

Figure 77: Experimental setup of supercapacitor module with bidirectional SMPS

5.6 Experimental Results

The hexa-mode converter is evidently able to charge the supercapacitor module without the implementation of hybrid state, as shown in Figure 78. The input voltage is deliberately tuned to fluctuate by controlling the voltage knob on the DC power supply. It is noted that at several instances, there are current spikes whilst fluctuating the DC voltage. This occurs

because the converter is oscillating between the buck-boost mode and boost mode. To avoid the occurance of spikes, the hybrid state has to be implemented.

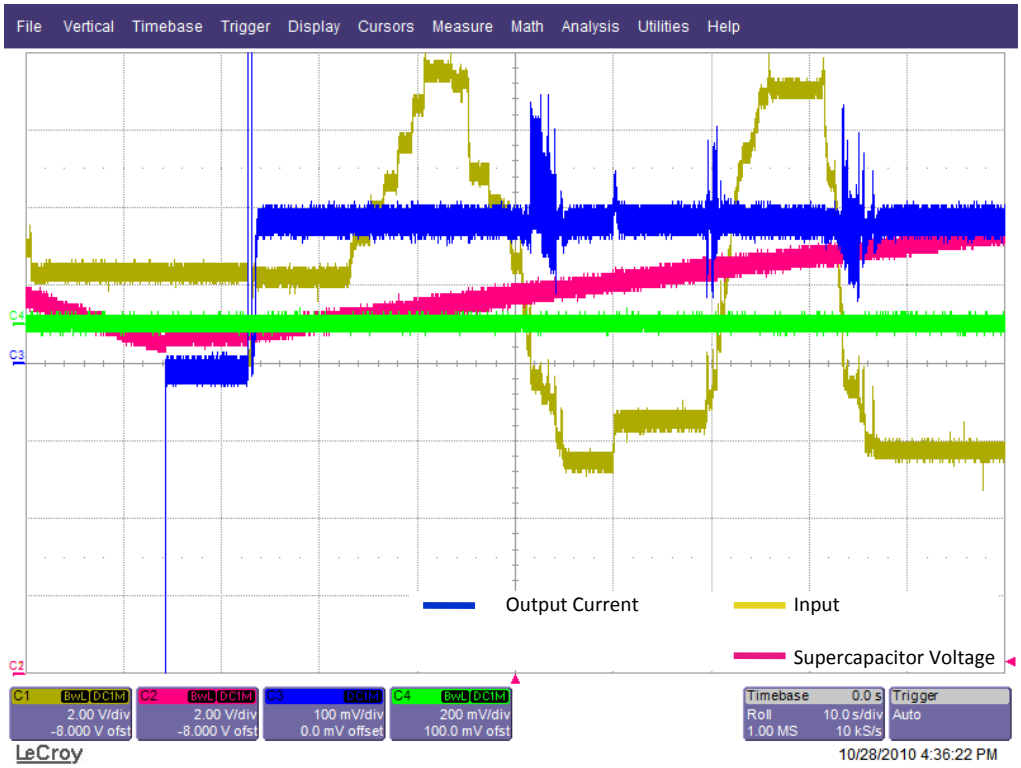

Figure 78: Performance of hexa-mode converter in constant current mode charging supercapacitor

Figure 79 shows the waveform of the hexa-mode converter with hybrid state. The charging current is consistent with no fluctuation throughout the whole charging range.

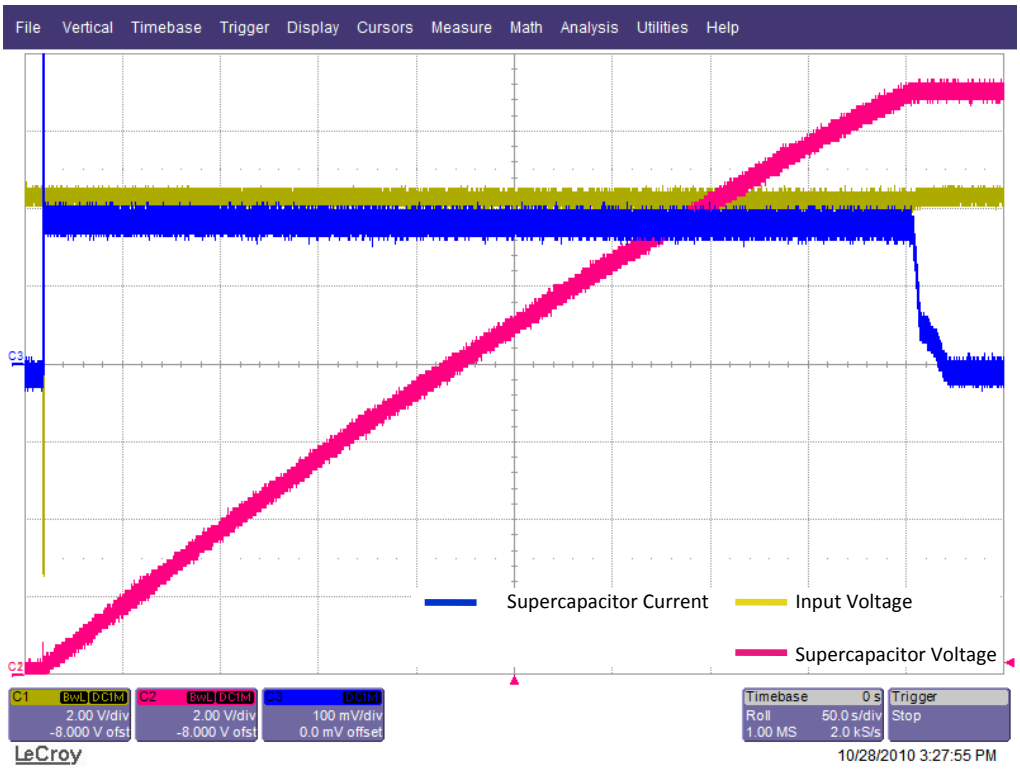

Figure 79: Waveform capture of the hexa-mode converter with 2A constant charge current, 12V input voltage

Figure 80 and Figure 81 shows the waveform of the converter discharging the supercapacitor in constant voltage mode. All the waveforms are captured using the Lecroy WavePro 6300A oscilloscope. The electronic load was set to operate in constant current mode. It is seen that for Figure 80, the converter can no longer sustain constant voltage mode when the supercapacitor voltage is 4V. The output voltage falls but the current is continuous. As observed in Figure 81, it is seen that below 2V, the converter can no longer sustain constant 5V output. As indicated by (23), the converter DC voltage gain is limited under a constant current load in the presence of parasitic.

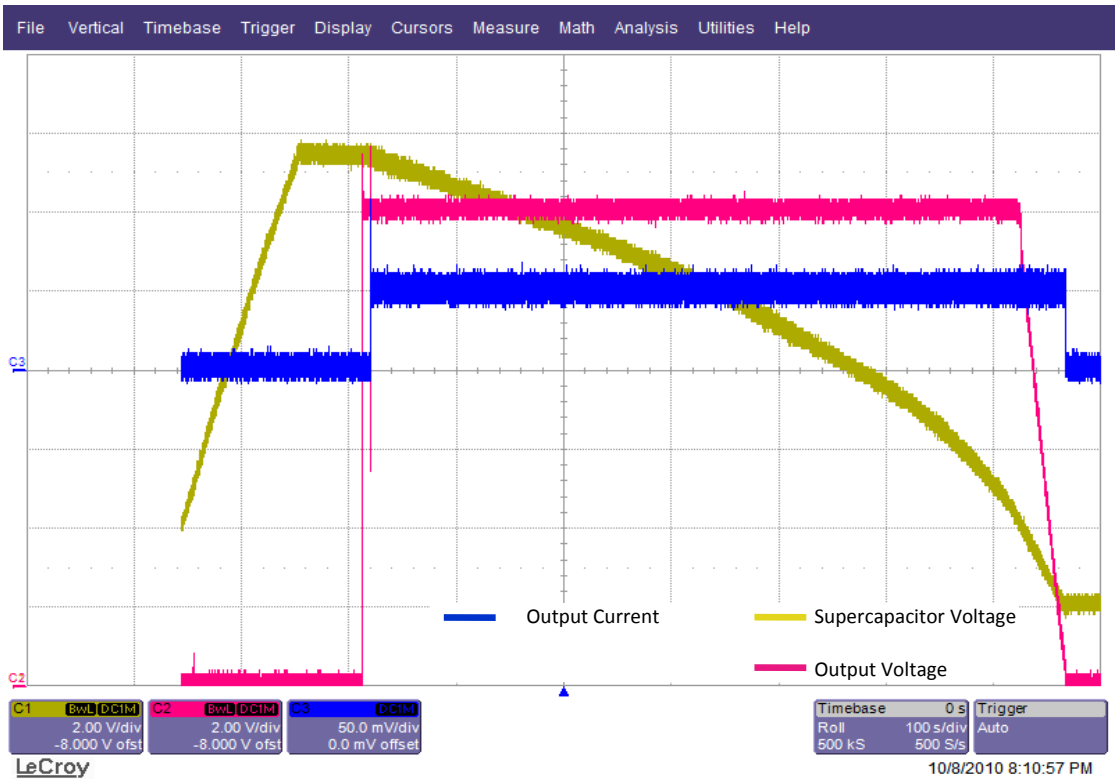

Figure 80: Waveform Capture of hexa-mode Converter with 3A constant current load, 12V output voltage

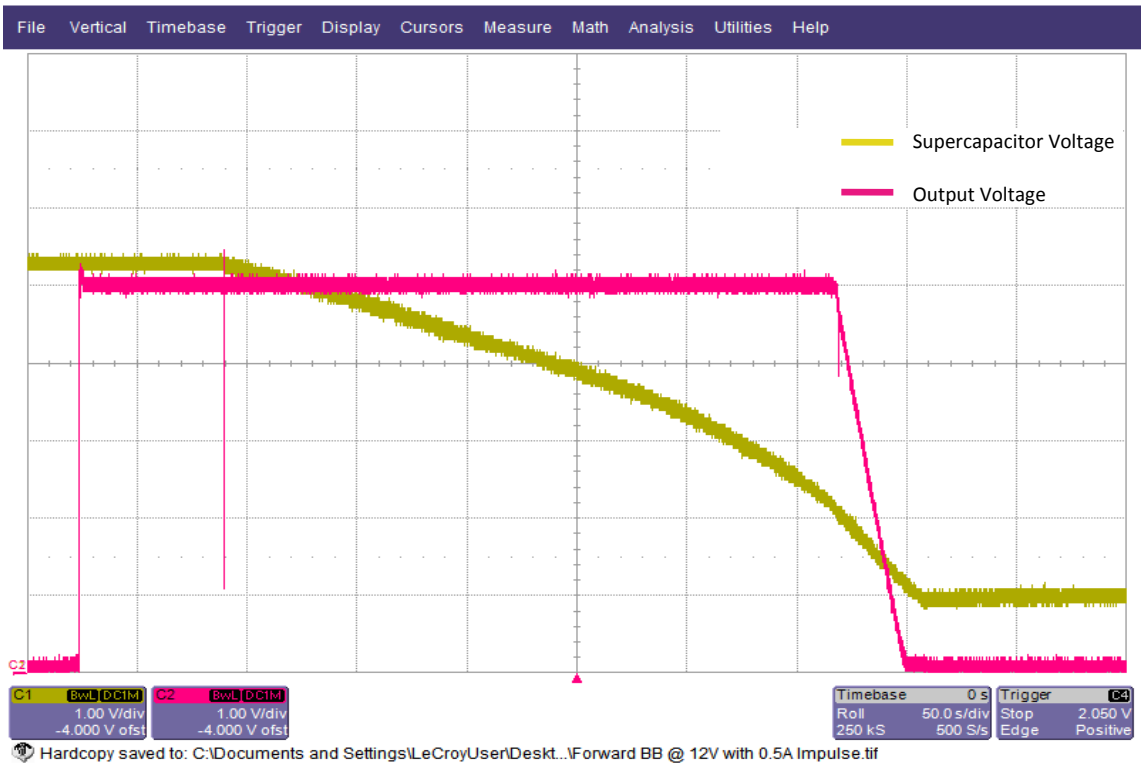

Figure 81: Waveform Capture of hexa-mode converter with 3A constant current load, 5V output voltage

Figure 82 shows the converter going into constant voltage mode without load, and after which an impulse current load is added. The converter is able to recover and handle the current impulse load.

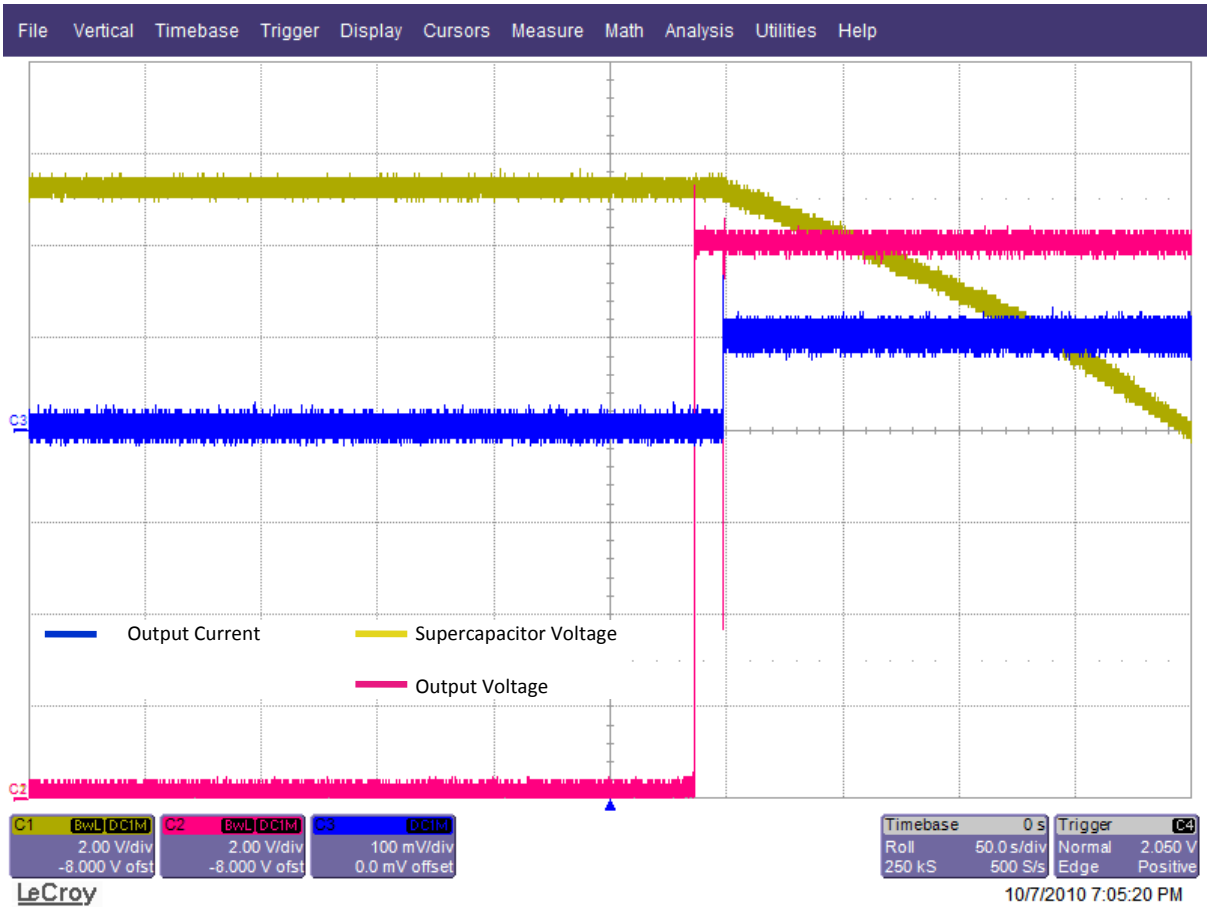

Figure 82: Converter performance during start up and impulse load

5.7 UPS Functionality

The peak load shaving capability can be modified to achieve a UPS purpose. When the original DC source was switched off, in this case a DC power supply, the SMPS came into operation by maintaining the voltage line. Many modern devices have use for such a device, such as [21]. A typical 3.5” Hard Disk Drive (HDD) consumes 0.5A at the 12V line while it

consumes 0.7A at the 5V line [39]. This prototype converter is more than sufficient to handle the requirements.

There are two methods to implement this function. The first links the DC power source directly to the supercapacitor. The hexa-mode converter takes the combination of both and regulates the output voltage to the desired voltage, as observed in Figure 83. This combination is known as the online UPS.

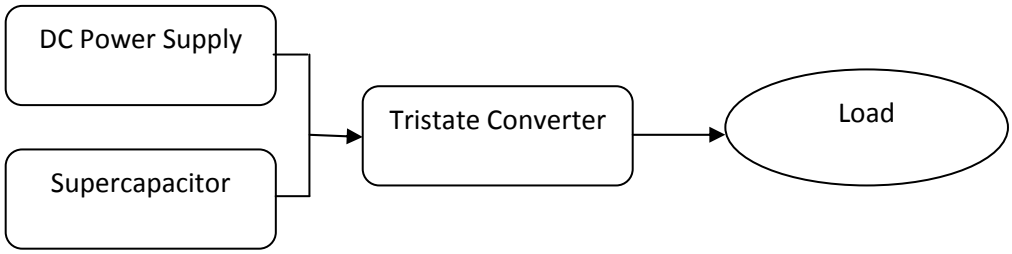

Figure 83: Online UPS implementation

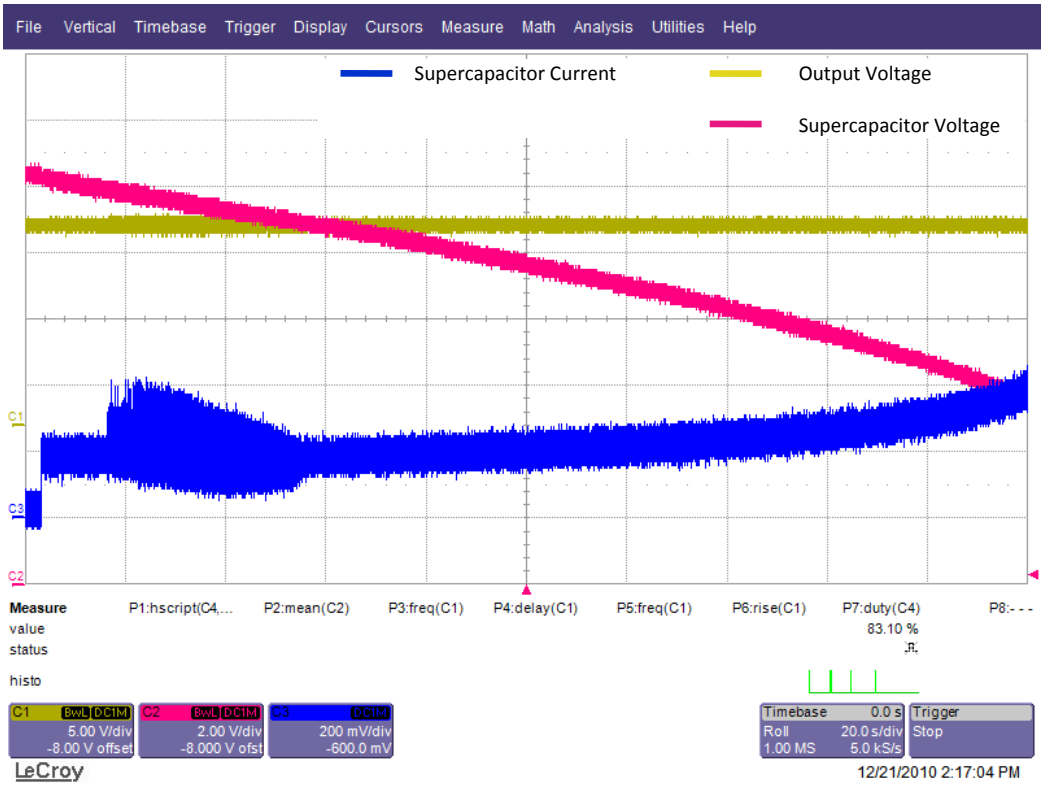

Figure 84: Seamless power delivery of the online UPS after the main DC source (power supply) was switched off

The second method implements the supercapacitor as an offline UPS, as observed in Figure 85 whereas the practical results are shown in Figure 86.

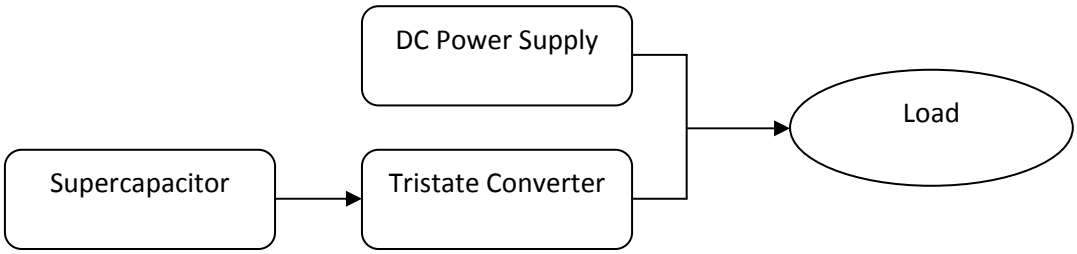

Figure 85: Offline UPS implementation

Figure 86: 0.12 seconds delay for the offline UPS voltage recovery

The practical experimentation to simulate source power loss was implemented by switching off the DC power supply while the UPS was in operation. The results of the offline UPS methodology was as shown in Figure 86. The online UPS method shows seamless power

delivery after the main DC source was switched off. The offline UPS method sees a maximum voltage dip of 5V but recovers in 0.12 seconds.

To simulate a poorly regulated source, the current limiter on the DC power supply was forced to fluctuate between 0.2A to 2.5A whilst the electrical load was set to be on a constant current load of 3A. To achieve voltage regulation, the hexa-mode converter has to supply current in counter fluctuating manner. Figure 87 shows the regulated voltage output and current output from both sources. It is observed that the output is regulated at 12V with little voltage fluctuation even though both sources undergo large fluctuation in current to deliver the 3A constant current demand.

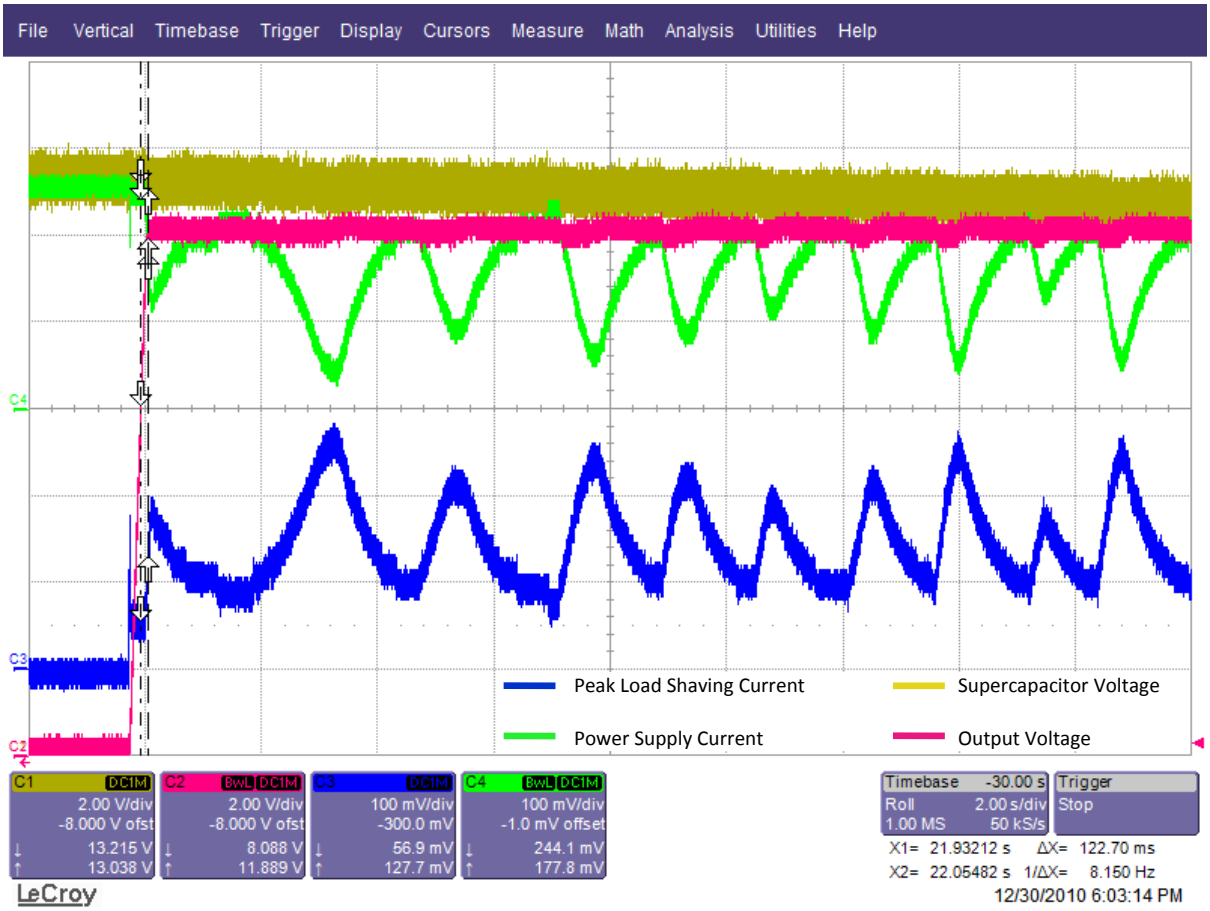

Figure 87: Active peak load shaving with fluctuating source

5.8 Application: Supercapacitor Based UPS in HDD Applications

With the hexa-state converter implemented and functionality proven, it is suitable for implementation to real applications. A 320GB 2.5” HDD from Western Digital Scorpio Blue series, rated at 5V 0.55A, was used as the specimen to implement data storage offline UPS.

Two 50F Maxwell supercapacitor were connected in series to offer a supercapacitor module of 5.4V for this application. The supercapacitor UPS was connected in parallel to the portable computer power supply, which is used to power the HDD. The HDD is also connected to the ASUSTEK P6T SE motherboard through the Serial ATA (SATA) interface so that data communication can take place. To check that the HDD is working fine, the portable computer power supply was turned on prior to turning on the computer. Upon booting to the Windows 7 Operating System (OS), the computer recognises the HDD, which were represented by partitions G: and H: local drives, as observed in Figure 88.

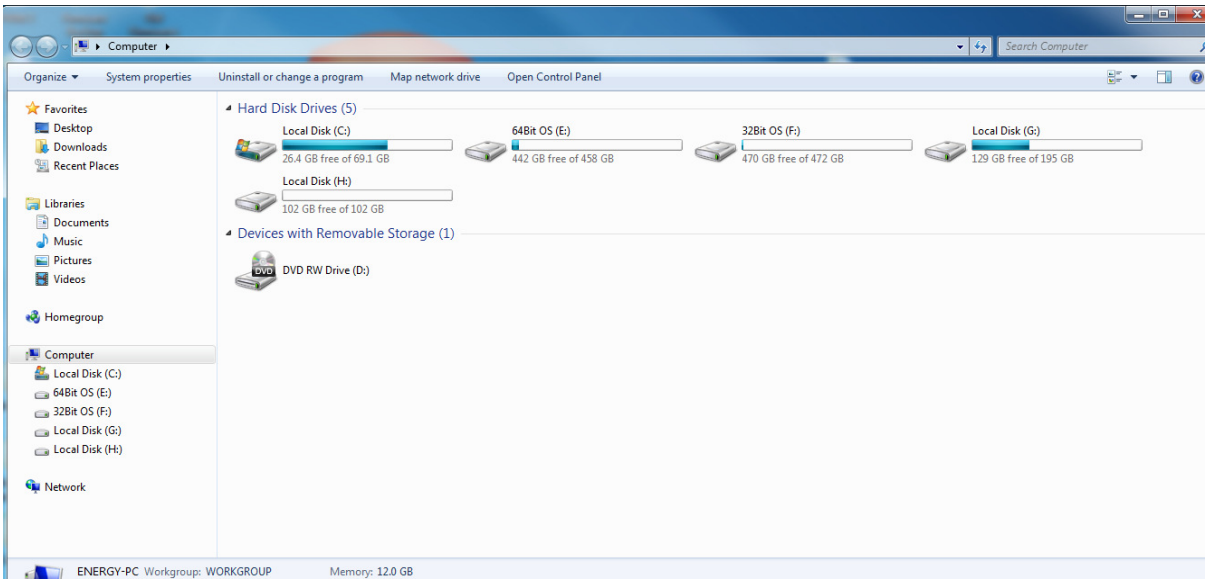

Figure 88: The HDD is detected by Windows denoted by G: and H: local drive

To observe the effect of power loss during data writing, the portable power supply was switched off through the mains switch whilst a folder of 2.58GB was made to write to the HDD, Windows prompted an error, as shown in Figure 89, which causes the removal of the two local drives. Windows did not register the two drives even after the mains switch was switched on and the HDD was operational again, as shown in Figure 90. This is due to the non plug-and-play operation of the SATA interface.

Upon system reboot, it was discovered that only 30% of data was intact: The rest has been lost due to the loss of electrical power. This has serious implications: If the UPS is not able to respond in time before the HDD powers down, the data is lost and the UPS would have lost its purpose. The disappearance of local drives from the Windows platform serves as a reliable check if the HDD has been powered down during the process of power recovery.

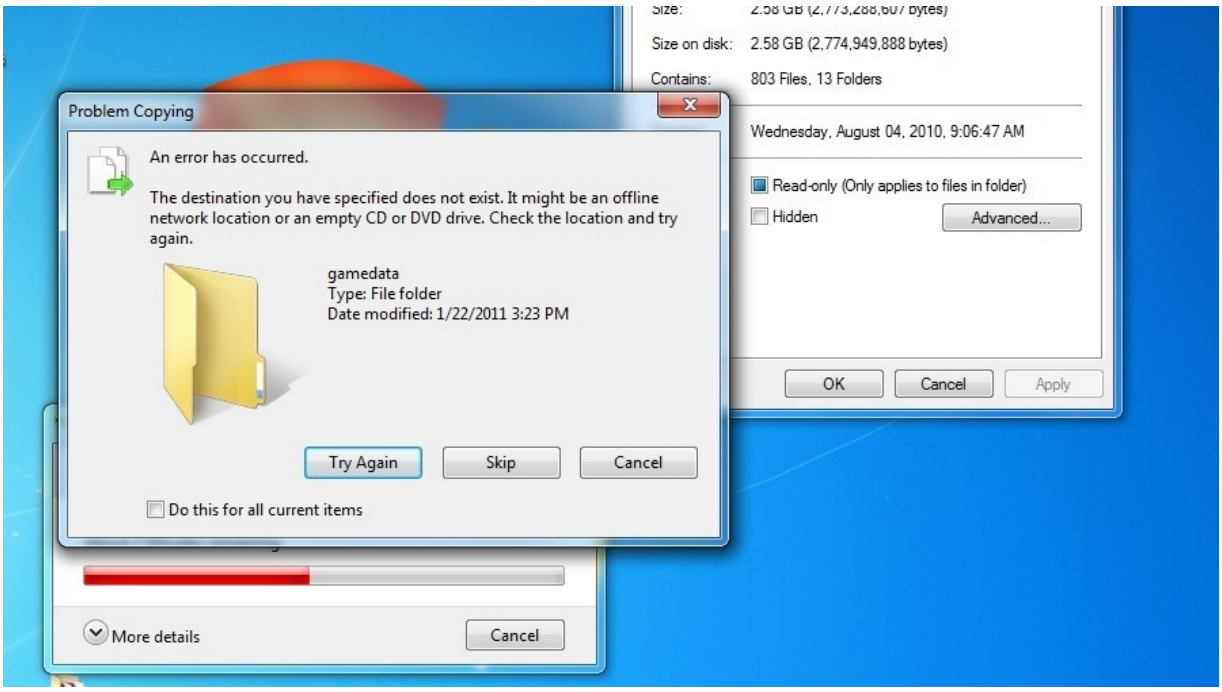

Figure 89: Windows prompt error on switching off power supply mains

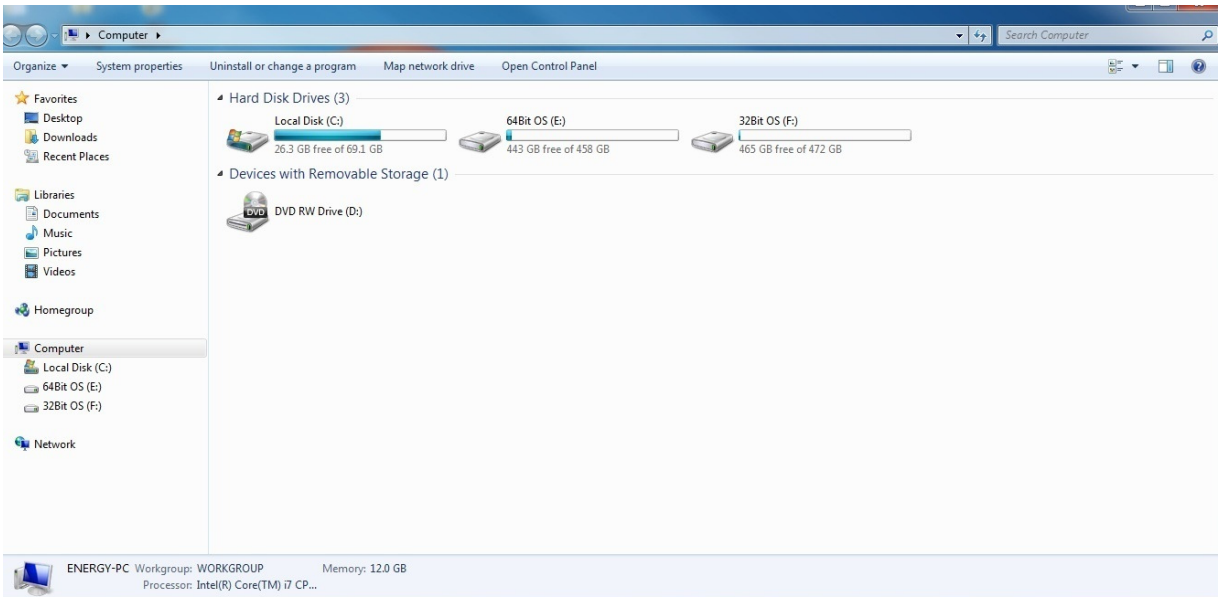

Figure 90: Windows unable to recognize local drives after re-powering the HDD

The experiment was then reinitiated, with the supercapacitor system operational as an offline UPS. Figure 91 shows the experiment setup while Figure 92 shows the voltage and current waveform of the system. The same 2.58GB of data was made to write to the HDD, and the portable power supply was switched off through the mains switch during so. It was noted that data transfer was not interrupted by doing so: The local drives were still detected and functional, while data transfer was completed with no data loss. This implies that the UPS functionality is successful and the HDD was not once powered down when the portable power supply was turned off. When the HDD is not powered down, the data in the volatile cache is intact.

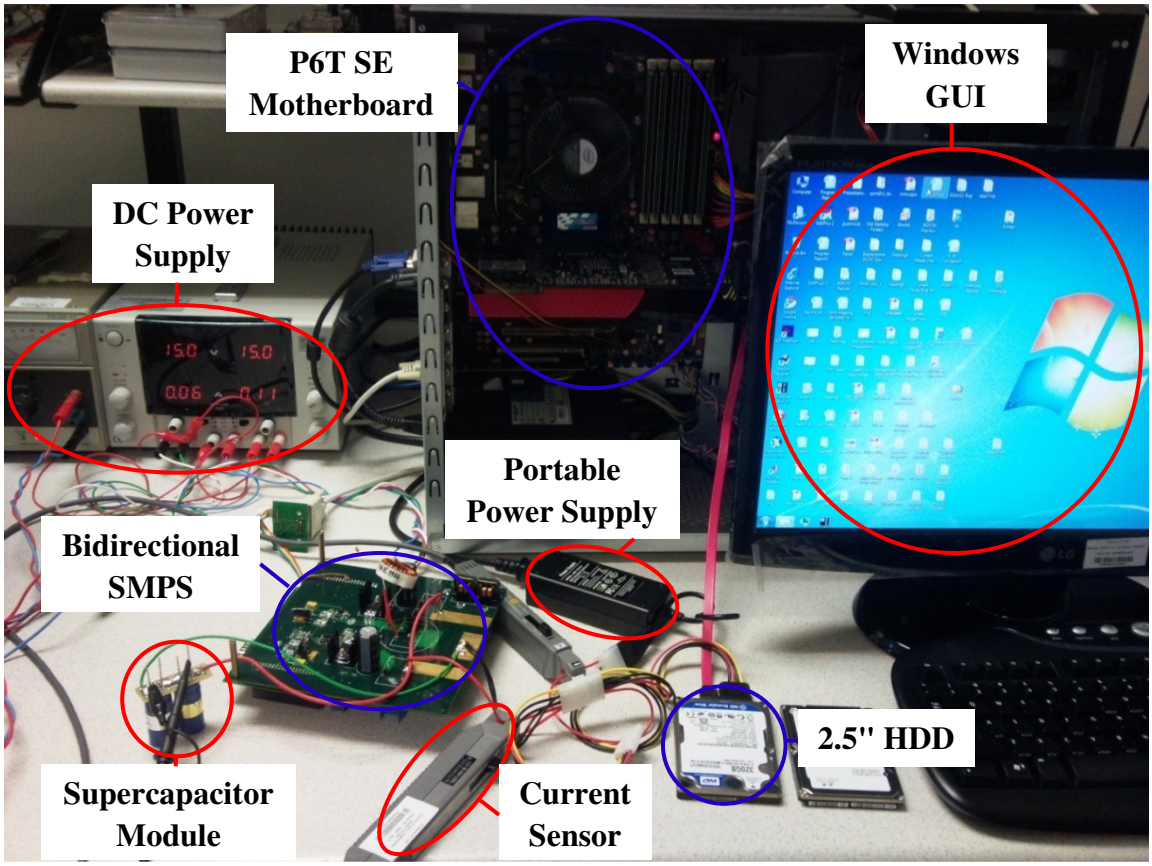

Figure 91: Supercapacitor offline UPS experimental setup

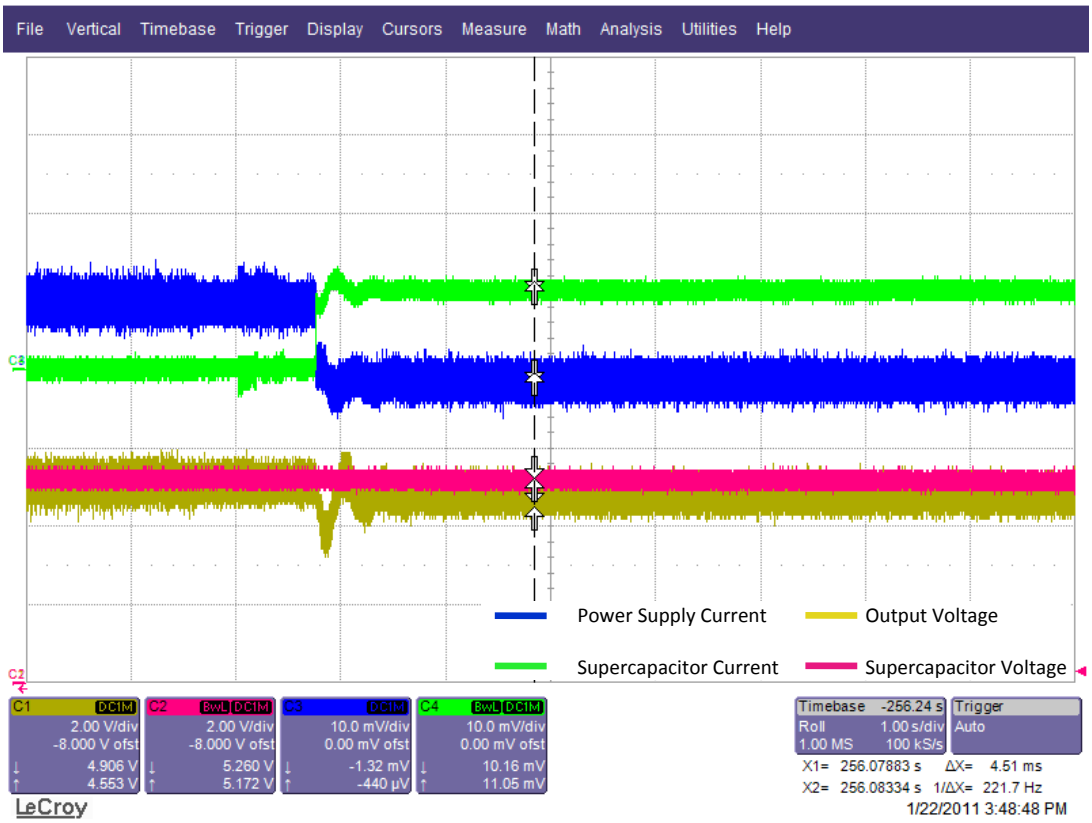

Figure 92: 5.4V supercapacitor UPS for 2.5” HDD

5.9 Chapter Conclusion

To add flexibility to the system, the hexa-mode converter has been implemented using the ADMC 401 DSP. The successful operation of the system is a testimony that the DSP algorithms are functional. The implementation of DSP allows the DSP to incorporate many functions not available using analog control. It is shown that the indirect sensing of output current using inductor current is effective in implementing the constant current control, which realizes the function of constant current charge of supercapacitor. The voltage mode is effective in maintaining voltage regulation in both offline UPS as well as active peak load shaving applications.

Data storage devices can benefit from an energy buffer, in the case that power loss occurs. The larger the cache, the more data loss is likely in the case of power failure. As there is a trend in increment of HDD and SSD cache, the energy buffer is important. It has been proven that using the offline supercapacitor UPS, one can prevent data loss due to the event of mains power loss. The application of the hexa-mode converter is vast and plentiful, and the supercapacitor based UPS used in HDD is only one of the many possible applications.

Chapter 6

Conclusions and Future Works

6.1 Background

This thesis describes the technologies in characterization and application of supercapacitor. The study is aimed at contributing to the understanding of supercapacitor and the issues related to supercapacitor application. A number of issues have been addressed and these issues reflect the developments in ideas leading towards:

i. Reliable acquisition of supercapacitor parameters

ii. Supercapacitor modeling

iii. Versatility in implementation of supercapacitor

6.2 Reliable Acquisition of ESR - Unification of AC and DC ESR

Four methods of supercapacitor ESR measurement techniques are presented. The research shows that DC ESR should be acquired by using constant current pulse method. EIS is the only equipment to obtain the AC ESR. During the constant current pulse experimentation, it was discovered that the supercapacitor terminal voltage does not fall linearly with constant current discharge. This deviation generate nonlinear characteristic in time domain, resulting in the corresponding difference in DC ESR values as well. By acknowledging that the constant current pulse is equivalent to the half-period of an AC cycle where the

supercapacitor discharges, it is reasonable to convert the DC ESR to the frequency domain by doubling the time interval in which the gradient is obtained. On comparing the AC ESR at the same frequency as the DC ESR, it is shown that the AC ESR is indeed comparable to the DC ESR.

Thus, the AC EIS topology can be used to obtain DC ESR by operating in the corresponding low frequency. This allows both manufacturers and researchers to use EIS methodology to obtain both DC and AC ESR in a single experimental setup, as compared to setting up two sets of equipments for measuring both data. In addition, this method offers a non-invasive method to acquire charged supercapacitor ESR without the need to charge or discharge it. On the other hand, the constant current pulse method requires a DC constant current flow which is considered invasive as it affects the supercapacitor voltage rating. Using the AC EIS methodology to obtain DC ESR can reduce the hassle for users to monitor the SOH of the supercapacitor in existing equipments. Therefore, there should not be terms such as AC ESR and DC ESR. There should be only an ESR with respect to frequency.

6.3 Supercapacitor Modeling - Modified RC Model

Several supercapacitor models are presented, whilst agreeing that the multi-branch model is able to describe both the supercapacitor dynamic and long term static behavior by taking into consideration the redistribution effect. The voltage regulator is in idle state when the supercapacitor is undergoing redistribution. Thus, this allow us to solely consider the single RC branch model, which is significantly simpler compared to the multi-branch model. However, the basic RC branch model was unable to replicate the non-linear voltage increment due to constant current charge. Thus, parameters such as $K_C(V)$ and $K_V(V)$ are

added to the basic RC model to reflect the change in capacitance and ESR with voltage respectively. This model is therefore termed the modified RC model.

Through simulation of the modified RC model, which takes into account the change in capacitance and ESR with regards to voltage, the results matches well with the experimental values where dynamic behavior is concerned. This proves that the deviation of voltage linearity under constant current charge/discharge is attributed more to the change in capacitance. This presents a single RC branch model that reflects better dynamic behavior compared to that of the basic RC model.

6.4 Application of the Supercapacitor - Hexa-Mode Converter

The bidirectional hexa-mode converter was chosen to complement the implementation of supercapacitor. This is in particular, important to supercapacitor whose voltage is above that of the output voltage. Operation in the buck-boost mode allows flexibility for the supercapacitor to operate at voltages higher or lower than its output voltage. However, the DC voltage gain ratio was limited due to the presence of parasitic. Therefore, the boost mode has to be activated when the buck-boost mode was unable to meet the DC voltage gain ratio requirements, typically when the supercapacitor voltage is low compared to the output voltage.

It was discovered that oscillations happened in the operation at the boundary of the buck-boost mode and the boost mode. To ease the transition, a hybrid state which bridges both the buck-boost and boost mode is introduced. The hybrid state converter promises higher DC voltage transfer ratio then the buck-boost mode. As a matter of fact, the hybrid state resumes operation of the buck-boost and boost mode when $\alpha = 0$ and α = 1-D respectively.

Experimental waveforms indicate that the transition from buck-boost to the hybrid state and then to the boost state is seamless and suffers no oscillation. The methodology developed is suitable to implement applications such as robust UPS for hard disk drive as well as regenerative braking system in EVs.

6.5 Future Works

Some ideas possible for future implementation are as listed:

1. The hexa-mode converter power capability can be further developed. Higher voltage and current operation is possible by upgrading the key components to accommodate the upgrade. Components such as inductor and MOSFET switches with ultra low ESR can be used to minimize parasitic loss and maximize DC voltage transfer ratio. Some of the newest MOSFETs with unique packaging can achieve an ESR being lower than 1mΩ. All of these improve SMPS efficiency which is crucial to preventing thermal runaway when higher power transfer is taking place. With the same topology but different components, higher power is possible. Operation in the range of 1-10kW range is likely to be possible.
2. Characterization of the pseudo-capacitor is advantageous, as it offers more energy density compared to that of EDLC. Pseudo-capacitor is likely to have more applications in comparison to EDLC, and therefore development of effective transient modeling of the pseudo-capacitor is necessary. It is expected that the EIS is going to be effective for the pseudo-capacitor, like in the case of EDLC.

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List of Publications Associated to this Research Work

Paper under Review:

1. Ng Aik Thong, Bi Chao, Jiang Quan and Hong Ming Hui, ”Novel Method of Obtaining Supercapacitor DC ESR from AC Acquisition Methods”, 2011 IEEE Vehicle Power and Propulsion Conference

Appendix A

HEXA-MODE BUCK-BOOST CONVERTER: DERIVATION OF SMALL-SIGNAL TRANSFER FUNCTION MODEL

A.0 Background

Chapter 4-5 discusses the hexa-mode buck-boost converter. The derivation in this section is used to demonstrate proof of concept simulation in chapter 4. This section presents the complete derivation for the small signal model as well as converter state functions taking into account the effect of system parasitic.

A.1 Complete Transfer Function – Derivation

Considering the hexa-mode converter in Figure 59, the following parasitic in the converter are considered.

$\mathrm{R_L} = \text{Inductor ESR}$

$\mathrm{R_{on}} = \text{MOSFET ON Resistance}$

$\mathrm{R_C} = \text{Capacitor ESR}$

$\mathrm{V_D} = \text{Diode Forward Voltage Drop}$

i_L denotes the average inductor current, $\mathrm{V_{In}}$ the source voltage, V_O the average output voltage, R the load resistance, V_C the average voltage across the filter capacitor, D the duty ratio and and α the duty ratio of the hybrid state.

During the D period, the state equations are described by

$$-\mathrm{V_{in}} + \mathrm{i_L R_L} + 2\mathrm{i_L R_{On}} + \mathrm{L}\frac{\mathrm{di_L}}{\mathrm{dt}} = 0 \quad , \tag{42}$$

$$i_C + i_O = 0 \quad , \tag{43}$$

and

$$C\frac{dV_C}{dt} + \left(\frac{V_C + CR_C \frac{dV_C}{dt}}{R} \right) = 0 \quad . \tag{44}$$

The state equation during the D period is therefore

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{2R_{On} + R_L}{L} & 0 \\ 0 & -\frac{a}{R \bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{In} \quad , \tag{45}$$

where $a = \frac{R}{R + R_C}$.

During the α period, the state equations are described by:

$$-V_{in} + i_L R_L + i_L R_{On} + L\frac{di_L}{dt} + V_D + V_O = 0, \tag{46}$$

$$i_C + i_O = i_L \quad , \tag{47}$$

and

$$C\frac{dV_C}{dt} + \left(\frac{V_C + CR_C \frac{dV_C}{dt}}{R} \right) = i_L . \tag{48}$$

The state equation during the α period is therefore:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{On} + R_L + a \bullet R_C}{L} & -\frac{a}{L} \\ \frac{a}{C} & -\frac{a}{R \bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{In} - \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_D \quad . \tag{49}$$

During the $1-D-\alpha$ period, the state equations are described by:

$$-i_L R_L + L\frac{di_L}{dt} + 2V_D + V_O = 0, \tag{50}$$

$$i_C + i_O = i_L \quad , \tag{51}$$

and

$$C\frac{dV_C}{dt} + \left(\frac{V_C + CR_C\frac{dV_C}{dt}}{R}\right) = i_L \quad . \tag{52}$$

The state equation during the $1-D-\alpha$ period is therefore:

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_L + a\bullet R_C}{L} & -\frac{a}{L} \\ \frac{a}{C} & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} - \begin{bmatrix} \frac{2}{L} \\ 0 \end{bmatrix} V_D \quad . \tag{53}$$

The average equation of the converter can be written as below:

$$\begin{aligned} \begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} &= \begin{bmatrix} -\frac{2R_{On} + R_L}{L} & 0 \\ 0 & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} \times D + \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{In} \times D + \begin{bmatrix} -\frac{R_{On} + R_L + a\bullet R_C}{L} & -\frac{a}{L} \\ \frac{a}{C} & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} \times \alpha \\ &+ \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_{In} \times \alpha - \begin{bmatrix} \frac{1}{L} \\ 0 \end{bmatrix} V_D \times \alpha + \begin{bmatrix} -\frac{R_L + a\bullet R_C}{L} & -\frac{a}{L} \\ \frac{a}{C} & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} \times (1-D-\alpha) - \begin{bmatrix} \frac{2}{L} \\ 0 \end{bmatrix} V_D \times (1-D-\alpha) \end{aligned} \tag{54}$$

The equation (54) can be simplified as ,

$$\begin{bmatrix} \frac{di_L}{dt} \\ \frac{dV_c}{dt} \end{bmatrix} = \begin{bmatrix} -\frac{R_{On}(2D+\alpha) + R_L + a\bullet R_C\bullet(1-D)}{L} & -\frac{a}{L}(1-D) \\ \frac{a}{C}(1-D) & -\frac{a}{R\bullet C} \end{bmatrix} \begin{bmatrix} i_L \\ V_C \end{bmatrix} + \begin{bmatrix} \frac{D+\alpha}{L} \\ 0 \end{bmatrix} V_{In} - \begin{bmatrix} \frac{2-2D-\alpha}{L} \\ 0 \end{bmatrix} V_D. \tag{55}$$

To obtain the small-signal model, perturbations are introduced in the control inputs ∝ and D (only one control input is perturbed at a time). This will cause a change in the dynamic variables I_L and V_C change. Let the perturbed variables be

$V_C = V_C + \check{V}_C, i_L = I_L + \check{I}_L, d = D + \check{D}.$

A.2 Derivation of D to State Transfer Functions

In this case, the control input α is constant. Applying the perturbed variables, we obtain:

$$\frac{dI_L + d\widetilde{I_L}}{dt} = -\frac{I_L + \widetilde{I_L}}{L}[R_{On}\left(2D + 2\widetilde{D} + \alpha\right) + R_L + R_C a\left(1 - D - \widetilde{D}\right)] - \frac{a}{L}\left(1 - D - \widetilde{D}\right)\left(V_C + \widetilde{V_C}\right) + \frac{D + \widetilde{D} + \alpha}{L}V_{In} - \frac{V_D}{L}(2 - 2D - 2\widetilde{D} - \alpha) \quad (56)$$

and

$$\frac{dV_C + d\widetilde{V_C}}{dt} = \frac{a}{C}\left(1 - D - \widetilde{D}\right)\left(I_L + \widetilde{I_L}\right) - \frac{a}{RC}(V_C + \widetilde{V_C}) \quad (57)$$

Removing the DC terms and neglecting the non-linear terms in the above equations, the small signal model can be obtained,

$$\frac{d\widetilde{I_L}}{dt} = -\frac{\widetilde{I_L}}{L}[\left(R_{On}\left(2D + \alpha\right) + R_L + R_C a\left(1 - D\right)\right] - \frac{a\widetilde{V_C}}{L}\left(1 - D\right) + \frac{\widetilde{D}}{L}[R_C a I_L - 2R_{On} I_L + aV_C + V_{In} + 2V_D] \quad (58)$$

$$\frac{d\widetilde{V_C}}{dt} = -\frac{a}{C}I_L\widetilde{D} + \frac{a}{C}\left(1 - D\right)\widetilde{I_L} - \frac{a}{RC}\widetilde{V_C} \quad (59)$$

Taking laplace transform, we have

$$sI_L\left(s\right) = -\frac{I_L(s)}{L}[\left(R_{On}\left(2D + \alpha\right) + R_L + R_C a\left(1 - D\right)\right] - \frac{aV_C(s)}{L}\left(1 - D\right) + \frac{D(s)}{L}[R_C a I_L - 2R_{On} I_L + aV_C + V_{In} + 2V_D] \quad (60)$$

and

$$sV_C(s) = -\frac{a}{C} I_L D(s) + \frac{a}{C}(1-D) I_L(s) - \frac{a}{RC} V_C(s) \quad . \tag{61}$$

V(s) can be eliminated from the equation above to derive the D to I_L transfer function:

$$\frac{I_L(s)}{D(s)} = \frac{(a^2(i_L(R-DR+Rc)+V_C)+CRs(-2i_L R_{on}+2V_d+V_{in})+a(-2i_L R_{on}+Ci_L RR_C s+CRV_c s+2V_d+V_{in})}{a^2(-1+D)((-1+D)R-R_C)+CRs(R_L+\alpha R_{on}+2DR_{on}+Ls)+a(R_L+(\alpha+2D)Ron+(L-C(-1+D)RR_C)s} \tag{62}$$

V_C and I_L can be related using by simplifying (60) and (61), that is,

$$V_C(s) = -\frac{(aD(s)i_L - aI_L(s) + aDI_L(s))R}{a+CRs} \tag{63}$$

and

$$I_L(s) = \frac{(a+CRs)V_C(s)}{aR(1-D)} + \frac{i_L D(s)}{(1-D)} \quad . \tag{64}$$

Also, eliminating $I_L(s)$ from the equation above, the D to V_C transfer function is:

$$\frac{V_C(s)}{D(s)} = -\frac{aR(i_L(R_L+(2+\alpha)R_{on}+Ls)+(-1+D)(aV_C+2V_d+V_{in}))}{a^2(-1+D)((-1+D)R-R_C)+CRs(R_L+\alpha R_{on}+2DR_{on}+Ls)+a(R_L+(\alpha+2D)R_{on}+(L-C(-1+D)RR_C)s)} \tag{65}$$

The output voltage V_O and capacitor voltage V_C are related by the following equation:

$$V_O = aR_C(1-D)i_L + aV_C \quad . \tag{66}$$

Substituting the perturbed variables to the equation above,

$$V_O + \widetilde{V_O} = aR_C\left(1-D-\widetilde{D}\right)\left(I_L+\widetilde{I_L}\right)+a(V_C+\widetilde{V_C})) \text{ .} \tag{67}$$

Neglecting the DC terms and performing laplace transformation, we get

$$\widetilde{V_O} = aR_C(1-D)\widetilde{I_L} - aR_C I_L \widetilde{D} + a\widetilde{V_C} \tag{68}$$

and

$$V_O(s) = aR_C(1-D)I_L(s) - aR_C I_L D(s) + aV_C(s) \quad \text{.} \tag{69}$$

Using (49), V_O reduces to

$$V_O(s) = \frac{aR_C(1-D)\left((a+CRs)V_C(s)+aRi_L D(s)\right)}{aR(1-D)}V_C(s) - aR_C I_L D(s) + aV_C(s)$$

$$= (1+sR_C C)V_C(s) \text{ .} \tag{70}$$

Thus, the overall D to V_O transfer function can be written as:

$$\frac{V_O(s)}{D(s)} =$$

$$-\frac{aR\left(i_L\left(R_L+(2+\alpha)R_{on}+Ls\right)+(-1+D)\left(aV_C+2V_d+V_{in}\right)\right)(1+sR_C C)}{a^2(-1+D)((-1+D)R-R_C)+CRs(R_L+\alpha R_{on}+2DR_{on}+Ls)+a(R_L+(\alpha+2D)R_{on}+(L-C(-1+D)RR_C)s)} \text{ .} \tag{71}$$

A.3 Derivation of α to State Transfer Functions

The control input *D* is held constant here. Applying perturbation variables, the following equations can be obtained:

$V_C = V_C + \tilde{V}_C$, $i_L = I_L + \tilde{I}_L$, $\alpha = \alpha + \tilde{\alpha}$,

$$\frac{dI_L + d\tilde{I}_L}{dt} =$$

$$= -\frac{I_L + \tilde{I}_L}{L}[R_{On}(2D+\alpha+\tilde{\alpha}) + R_L + R_C a(1-D)] - \frac{a}{L}(1-D)(V_C + \tilde{V}_C) + \frac{D+\alpha+\tilde{\alpha}}{L}V_{In} - \frac{V_D}{L}(2-2D-\alpha-\tilde{\alpha}) \quad (72)$$

and

$$\frac{dV_C + d\tilde{V}_C}{dt} = \frac{a}{C}(1-D)(I_L + \tilde{I}_L) - \frac{a}{RC}(V_C + \tilde{V}_C). \quad (73)$$

By removing the DC terms and neglecting the non linear terms, the small signal model is obtained below:

$$\frac{d\tilde{I}_L}{dt} = -\frac{\tilde{I}_L}{L}[(R_{On}(2D+\alpha) + R_L + R_C a(1-D)] - \frac{a\tilde{V}_c}{L}(1-D) + \frac{\tilde{\alpha}}{L}[-R_{On}I_L + V_{In} + V_D], \quad (74)$$

and

$$\frac{d\tilde{V}_C}{dt} = \frac{a}{C}(1-D)\tilde{I}_L - \frac{a}{RC}\tilde{V}_C \quad . \quad (75)$$

Using laplace transformation on (61) and (62), we have

$$sI_L(s) = -\frac{I_L(s)}{L}[(R_{On}(2D+\alpha) + R_L + R_C a(1-D)] - \frac{aV_C(s)}{L}(1-D) + \frac{a(s)}{L}[-R_{On}I_L + V_{In} + V_D], \quad (76)$$

and

$$sV_C(s) = \frac{a}{C}(1-D)I_L(s) - \frac{a}{RC}V_C(s) \quad . \quad (77)$$

The α to I_L transfer function can be computed as

$$\frac{I_L(s)}{\alpha(s)} = \frac{(-I_L R_{on} + V_d + V_{in})}{a(R_C - DR_C) + RL + \alpha R_{on} + 2DR_{on} + Ls + \frac{a^2(-1+d)^2 R}{a + cRs}} \cdot \quad (78)$$

V_C and I_L can be related using by simplifying (76) and (77), that is,

$$V_C(s) = \frac{aR(1-D)}{a + sRC} I_L(s) \quad , \quad (79)$$

and

$$I_L(s) = \frac{a + sRC}{aR(1-D)} V_C(s) \, . \quad (80)$$

The α to V_C transfer function can be denoted as

$$\frac{V_C(s)}{\alpha(s)} = \frac{a(1-d)R(-I_L R_{on} + V_d + V_{in})}{L(a + cRs)\left(\frac{aR_C - aDR_C + RL + \alpha R_{on} + 2DR_{on}}{L} + s + \frac{a^2(-1+d)^2 R}{L(a + cRs)}\right)} \, . \quad (81)$$

The output voltage V_O and capacitor voltage V_C are related by

$$V_O = aR_C(1-D)i_L + aV_C \quad . \quad (82)$$

Substituting the perturbed variables to the equation above, we have

$$V_O + \tilde{V}_O = aR_C(1-D)(I_L + \tilde{I}_L) + a(V_C + \tilde{V}_C) \quad (83)$$

Neglecting the DC terms and performing laplace transformation, it generates

$$\widetilde{V_O} = aR_C(1-D)\widetilde{I_L} + a\widetilde{V_C} \quad (84)$$

and

$$V_O(s) = aR_C(1-D)I_L(s) + aV_C(s) \quad . \quad (85)$$

Using (69), (68) reduces to

$$V_O(s) = \frac{aR_C(1-D)(a+sRC)}{aR(1-D)} V_C(s) + aV_C(s) = (1+sR_CC)V_C(s). \quad (86)$$

Therefore, the overall α to V_O transfer function can be written as

$$\frac{V_o(s)}{\alpha(s)} = \frac{a(-1+D)R(-I_LR_{on} + V_d + V_{in})(1+sR_CC)}{L(a+CRs)\left(\frac{aR_C - aDR_C + R_L + \alpha R_{on} + 2DR_{on}}{L} + s + \frac{a^2(-1+D)^2R}{L(a+CRs)}\right)}. \quad (87)$$

The DC Transfer function can be denoted as:

$$V_O = \frac{i_LR_L + \alpha i_LR_{on} + 2Di_LR_{on} + 2V_d - \alpha V_d - 2DV_d - \alpha V_{in} - DV_{in}}{(-1+D)}. \quad (88)$$

The ideal transfer function is denoted as:

$$\frac{V_O}{V_{in}} = \frac{\alpha + D}{(1-D)}. \quad (89)$$

It can be observed that when $\alpha = 1 - D$, the transfer function becomes that of the boost mode.

Appendix B

HARDWARE IMPLEMENTATION DETAILS OF THE HEXA-MODE BUCK-BOOST CONVERTER

B.0 Schematics of Hexa-Mode Buck-Boost Converter

This section shows the schematics of the hexa-mode buck-boost converter used for hardware implementation. The ADMC401 DSP master board is an intellectual property of Data Storage Institute, therefore the schematics of it will not be disclosed. Figure 93 shows the schematic for the converter power supply as well as the master board, while Figure 94 shows the DSP interface as well as the hexa-mode converter components. A number of components used in the daughter board was used to achieve optocoupler isolation between the control circuitry and the hexa-mode converter itself.

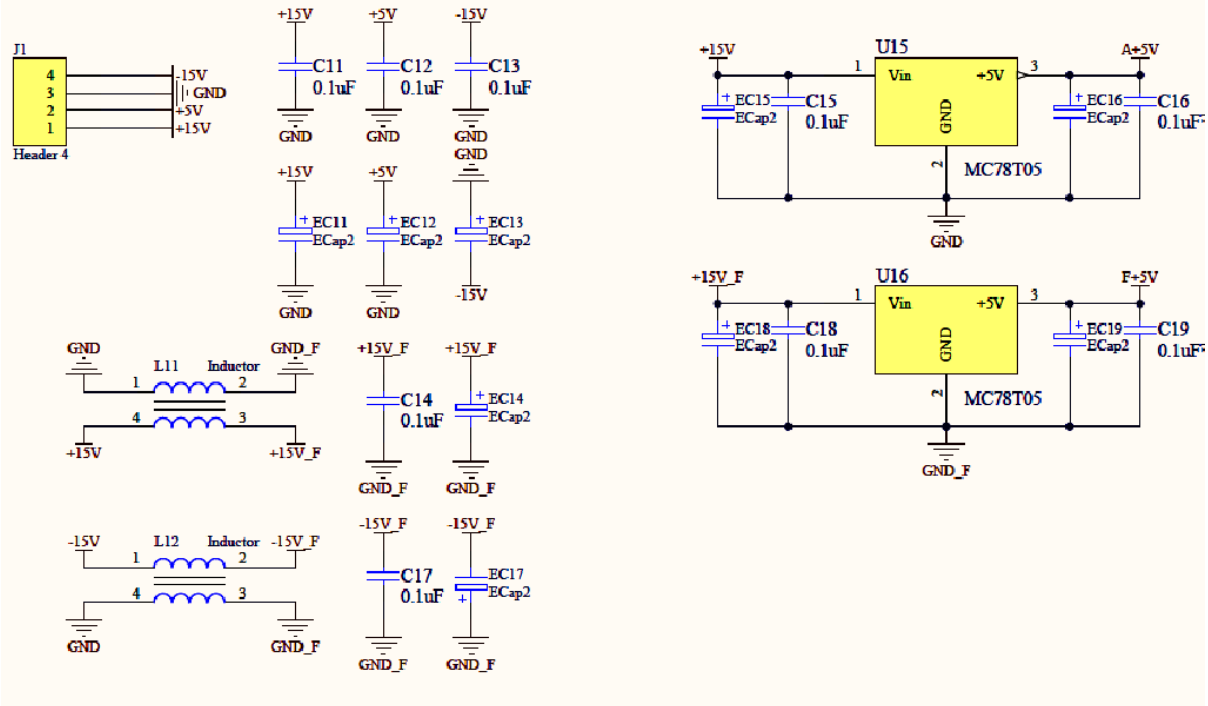

Figure 93: Schematic of daughter board power supply

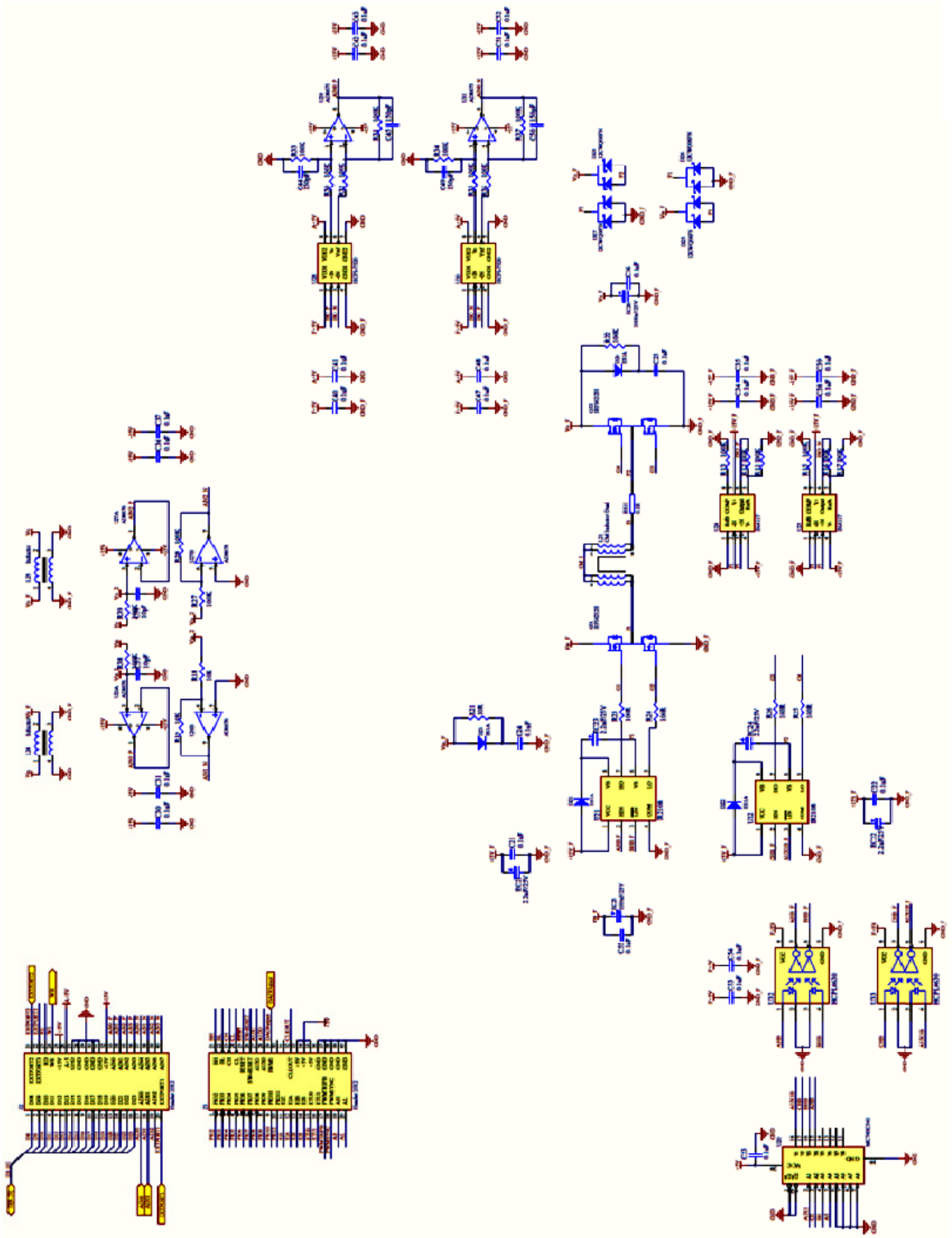

Figure 94: Schematic of daughter board with hexa-mode converter

Appendix C

Electronics Hardware Details for the Implementation of Supercapacitor Parameter Acquisition

C.0 Schematics of MOSFET Module with Integrated Current Sensor

This section shows and describes the schematics of the MOSFET module used for supercapacitor parameter acquisition, namely for the instantaneous voltage drop method as well as the constant current pulse method. The schematic was implemented on a 4 layer PCB, which allows good signal integrity.

The IR2127 is a generic bootstrap MOSFET driver that can drive majority of N-MOSFETs available commercially. As such, the MOSFET unit can be changed to allow higher voltage/current operation, though the PCB physically limits the N-MOSFETs footprint to TO-220 footprint. The sampling resistor RS401 and differential amplifier U402 provides the current sensing required. The sampling resistor can take on different values depending on the amount of current flowing through it. Figure 95 shows the schematic of the MOSFET module while Figure 96 shows the assembled MOSFET module.

Implementation of the MOSFET module was so convenient that the first hexa-mode SMPS prototype was built using it, as observed in Figure 97.

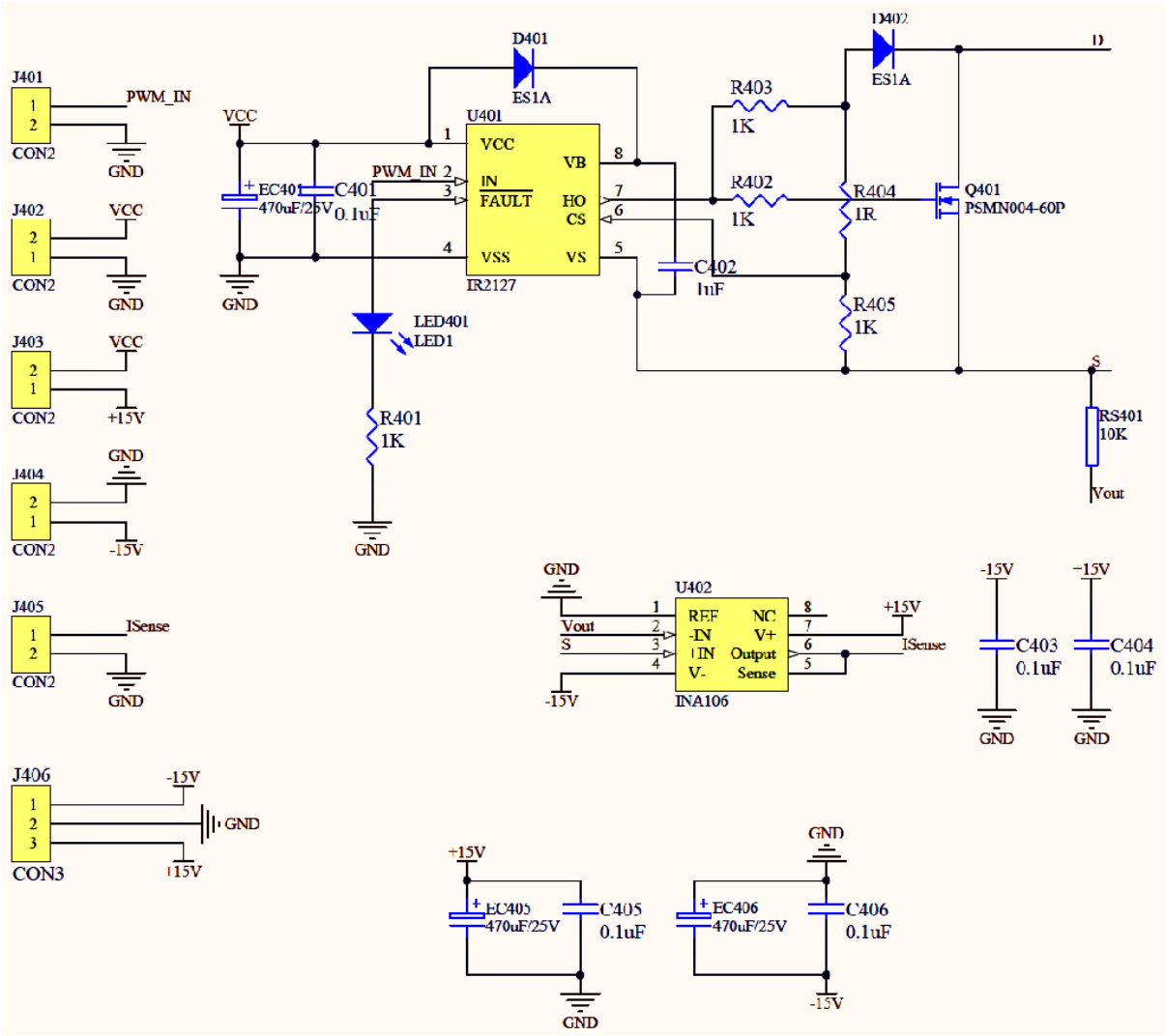

Figure 95: Schematics of MOSFET Driver with Integrated Current Sensor

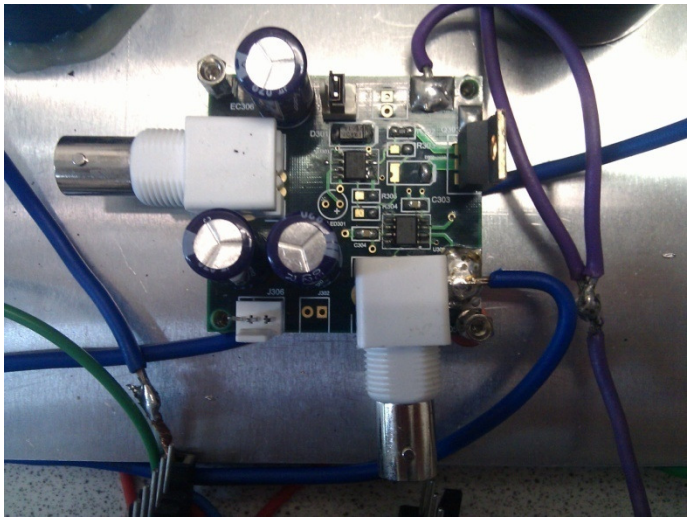

Figure 96: The MOSFET module: MOSFET driver with MOSFET with current sensor

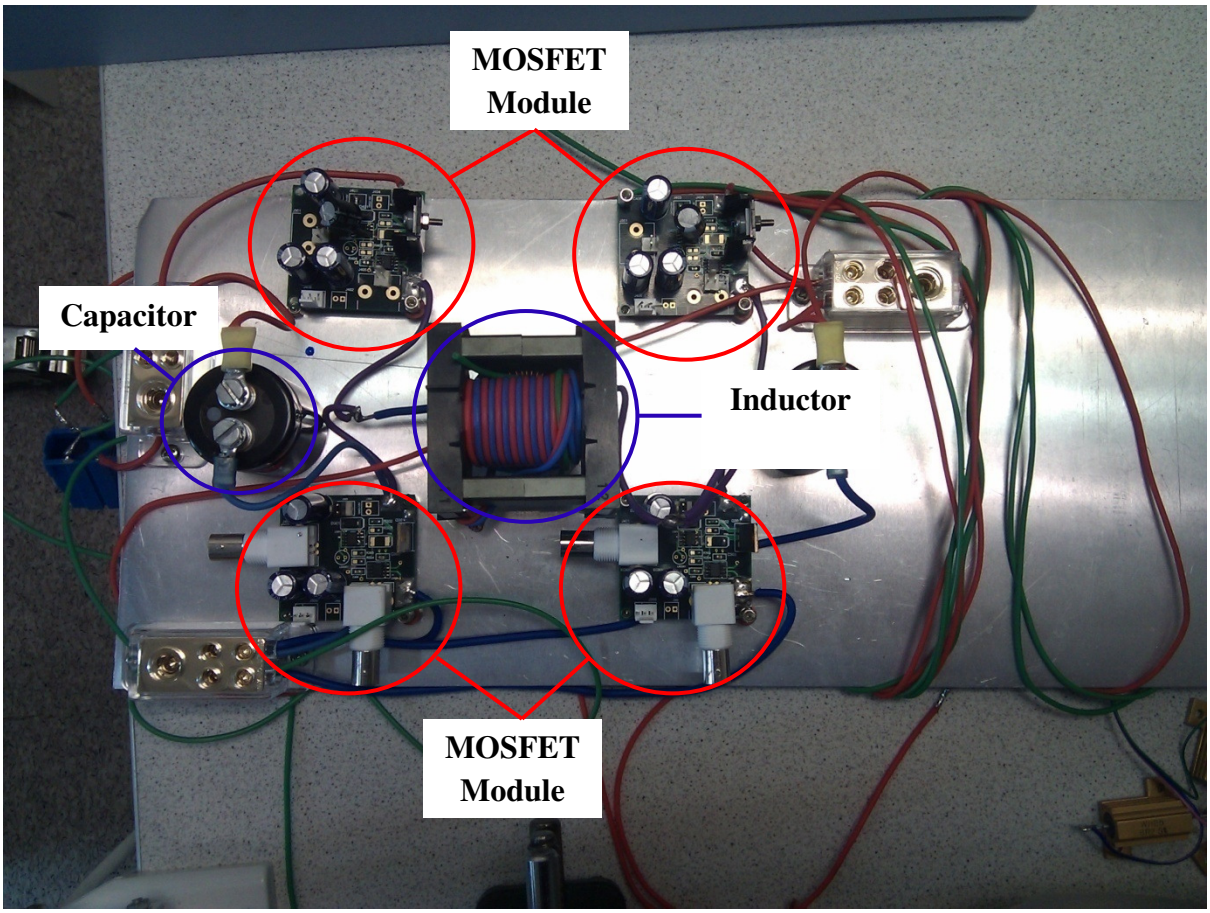

Figure 97: Hexa-mode converter prototype built using MOSFET modules